Product Specification

RS3263 Wideband Bypass LNA

General Description

The RS3263 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 1.95 GHz, the amplifier typically 18 dB gain, +35 dBm OIP3, and 1.3 dB noise figure while drawing 70 mA current from a +5 V supply. The component also provides high linearity in the bypass mode with +40 dBm IIP3. The RS3263 is internally matched and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature. The RS3263 covers the 0.6 – 4.2 GHz frequency band and is targeted for wireless infrastructure. The RS3263 is packaged in a 2 x 2 mm DFN

Applications

- 2G/3G/4G mobile infrastructure
- Repeater/DAS
- General purpose RF
- TDD/FDD system

Features

- Wideband
  - 0.6 – 4.2 GHz operational frequency
- Balanced performance in small package
  - 18dB Gain
  - 35dBm OIP3
  - 1.3 dB Noise Figure
  - 70mA current consumption under 5 V
  - 2 x 2 mm DFN package

Functional Diagram/Application Circuit

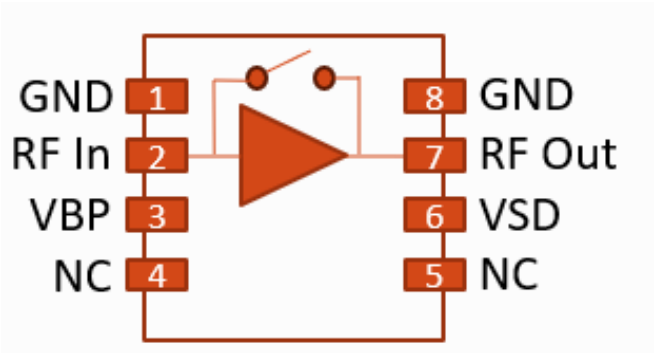


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
VDD to GND	-0.3	6	V
SD pin to GND	-0.3	6	V
Input Power, CW signal		20	dBm
Maximum Junction Temperature		175	°C
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM (Per JESD22-A114)		TBD	
ESD Voltage – CDM (Per JESD22-C101)		TBD	

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Recommended Operating Conditions

Table 2

Parameter	Min	Typical	Max	Unit
Supply Voltage (All VDD)	3	5	5.25	V
Operating Temp Range	-40	25	105	°C
Control Logic High Voltage	1.17	3.3	5	V
Control Logic Low Voltage	0		0.63	V
Input Power, CW signal			18	dBm

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

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Specification

Typical Application Circuit, VDD=5V, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 3

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		4200	MHz
Gain	700MHz		21		dB
	1800MHz		18		
	2500MHz		17.5		
	3600MHz		16.5		
	4200MHz		16.5		
Insertion Loss	700MHz		-1.4		dB
	1800MHz		-1.3		
	2500MHz		-1.5		
	3600MHz		-2.1		
	4200MHz		-1.8		
Input Return Loss	LNA mode or bypass mode		-11	-10	dB
Output Return Loss	LNA mode or bypass mode		-11	-7	dB
Output P1dB	LNA mode		17.5		dBm
Output IP3	LNA mode, Pout = 0 dBm/tone, Spacing = 1 MHz @2.5GHz		35		dBm
Input IP3	Bypass mode, Pout = 0 dBm/tone, Spacing = 1 MHz @2.5GHz		40		dBm
Noise Figure	700MHz		0.7		dB
	1800MHz		1.2		
	2500MHz		1.2		
	3600MHz		1.5		
	4200MHz		1.7		
Device Current, IDD	ON, Normal operation, VSD = 0 V		70		mA
OFF, Shut down, VSD = 1.8 V			4		mA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			150		μA
Device ON or OFF Timing, bypass or gain timing	50% of VSD to 90% or 10% RF Output		0.5	1	μs
Thermal Resistance, θjc	Junction to case		TBD		°C/W

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Pin Diagram

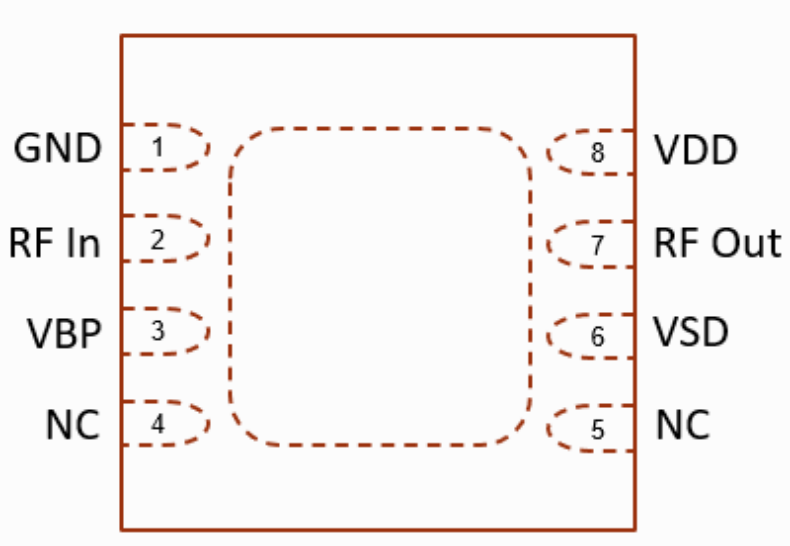


Figure 2

Pin Description

Table 4

Pad No.	Label	Description
1	GND	Ground
2	RFIN	RF Input. Requires a DC-blocking capacitor and an inductor.
3	Bypass	Control pin for bypass mode
4, 5	NC	NC. Recommend connect to PCB ground
6	Shutdown	Control pin to enable the LNA
7	RFOUT	RF Output. RFOUT is internally matched to 50Ω and incorporates an internal DC-blocking capacitor.
8	VDD	Voltage supply pin

Control Logic

Table 5

Mode	Bypass Pin	Shutdown Pin
LNA ON, Bypass OFF	0	0
LNA OFF, Bypass OFF	0	1
LNA OFF, Bypass ON	1	x

Application Circuit

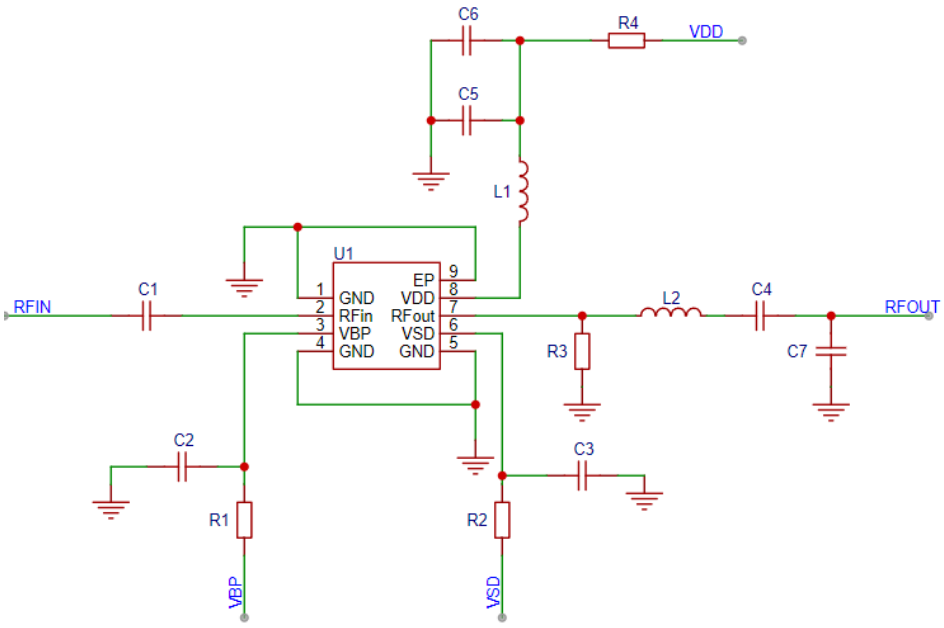


Figure 3

Table 6

Reference Designator	Value	Description
R1, R2, R4	0Ω	C0402
R3, C7	\	C0402
C1, C4	100pF	C0402
C2, C3	10pF	C0402
C5	1nF	C0402
C6	1uF	C0402
L1	16nH	C0603
L2	0Ω	C0402
U1	\	RS3263

Typical Performance Characteristics(LNA mode)

Figure 4. Gain

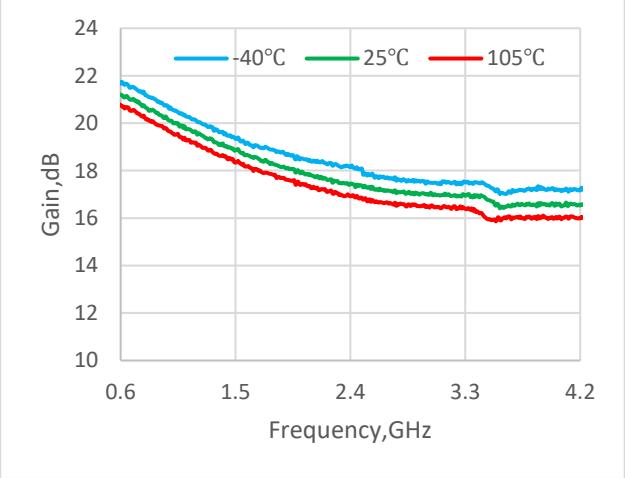


Figure 5. Input Return Loss

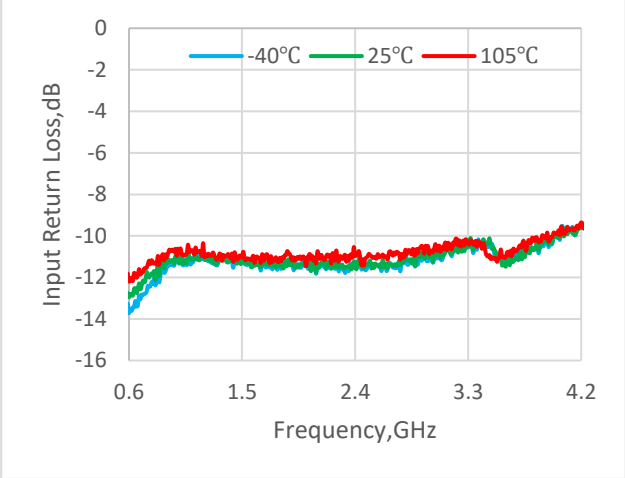


Figure 6. Output Return Loss

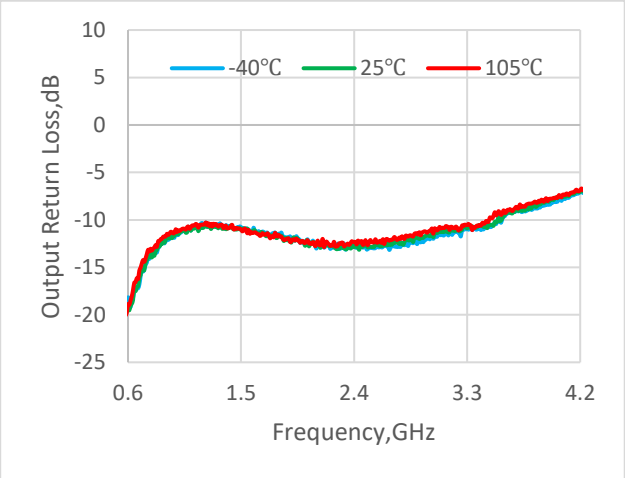


Figure 7. Noise Figure

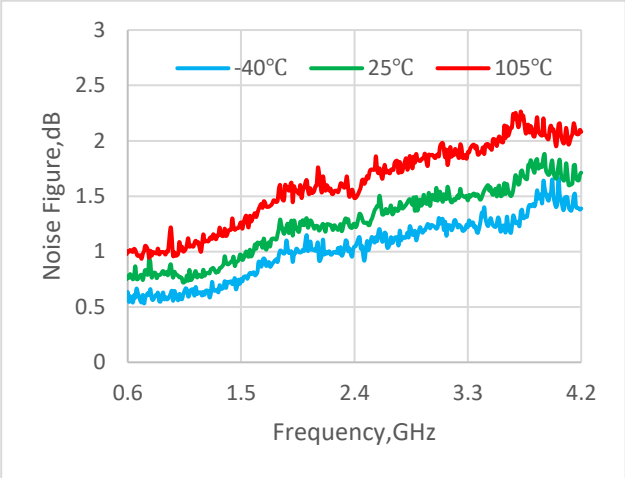


Figure 8. P1dB

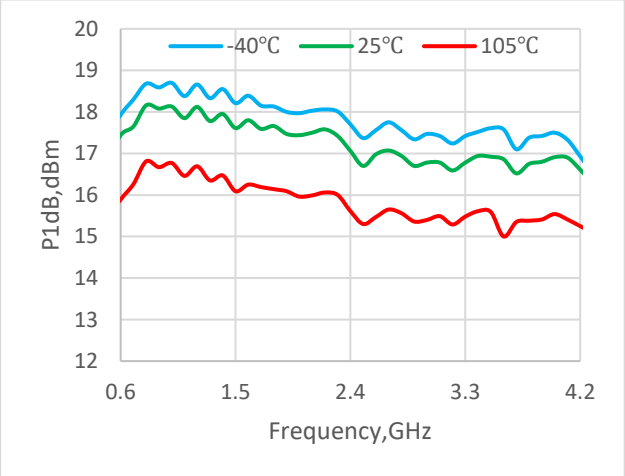
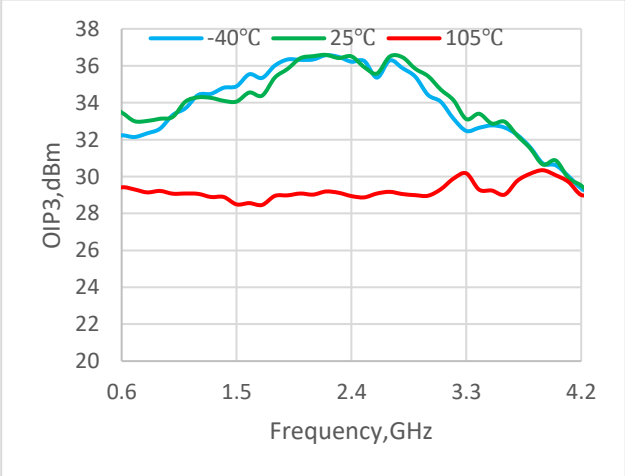


Figure 9. OIP3



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Typical Performance Characteristics(Bypass mode)

Figure 10. Insertion Loss

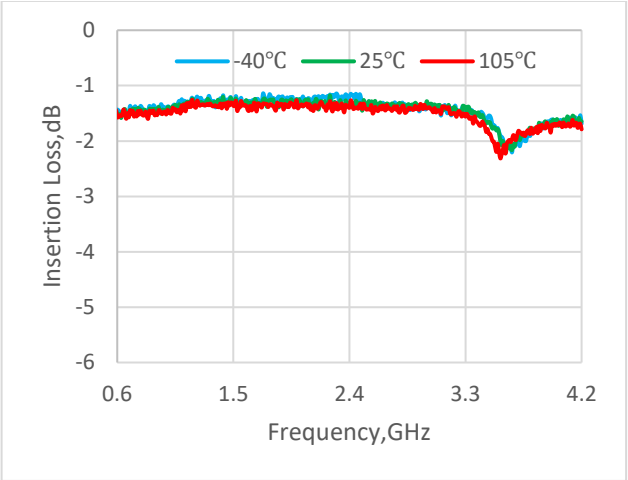


Figure 11. Input Return Loss

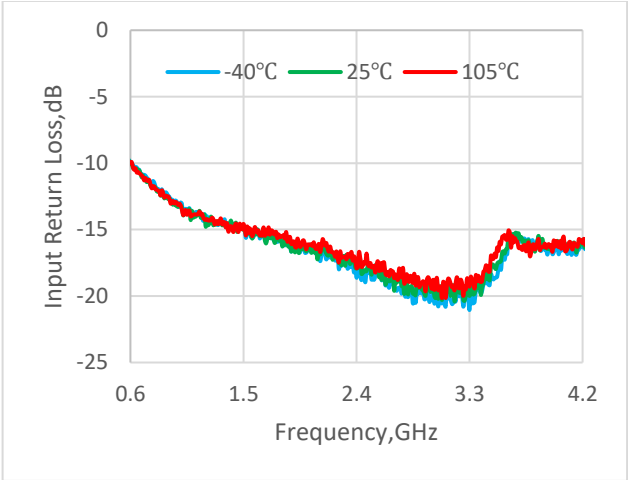


Figure 12. Output Return Loss

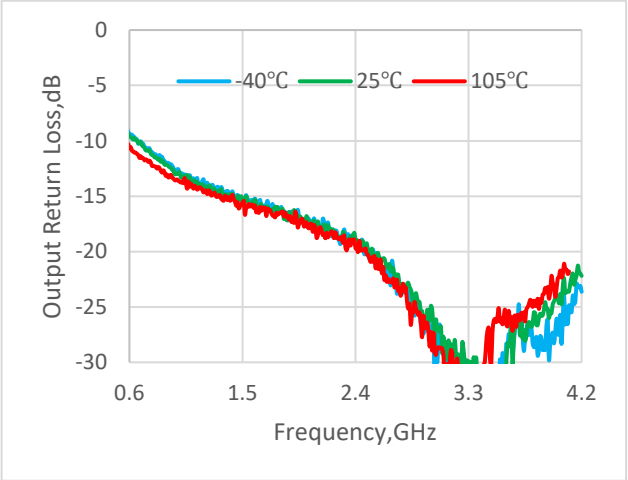


Figure 13. P1dB

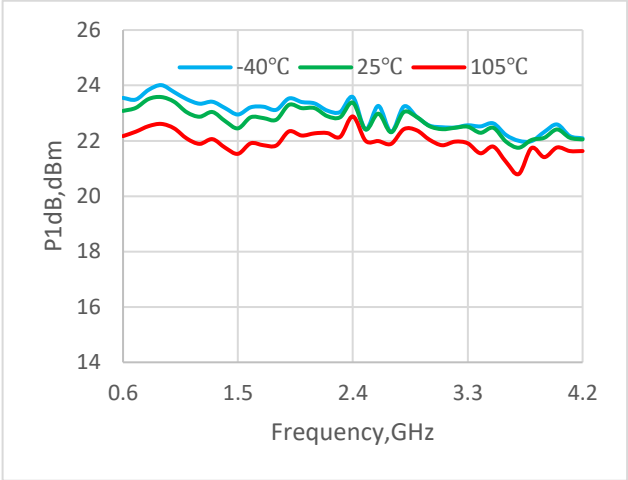
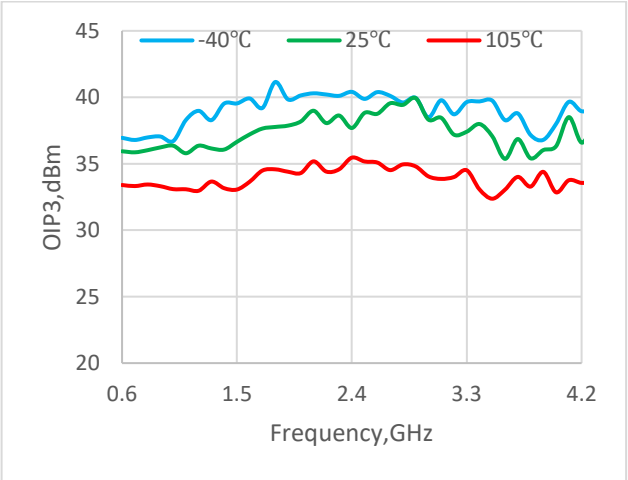
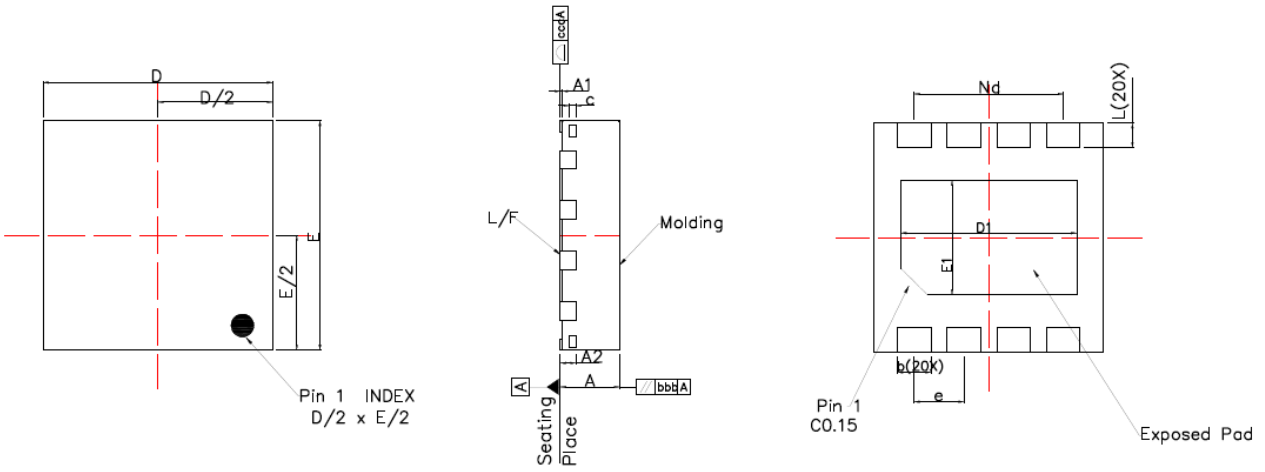


Figure 14. IP3



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Package Drawing



Dimensional References							
Ref.	MIN	NOR	MAX	Ref.	MIN	NOR	MAX
A	0.70	0.75	0.80	D1	1.65	1.70	1.75
A1	0	0.02	0.05	E1	0.95	1.00	1.05
A2		0.20 BCS		L	0.29	0.30	0.31
e		0.5 BCS		b	0.20	0.25	0.30
Nd		1.50 BCS		c			
Ne				aaa			
D	1.95	2.00	2.05	bbb			
E	1.95	2.00	2.05	ccc			

Note
1.All dimension are in millimeter.
2.Dimention 'A' includes package warpage.
3.Plating thickness 300 ~800 uinch

Figure 15

Revision History

Table 7

Revision Number	Revision Date	Description	Modifications
0.1	2022/7/25	Draft	—
0.2	2025/06/03		General Description/Features/Functional Block Diagram/Absolute Maximum Ratings/Specification/Pin Diagram /Applications Information/ Typical Performance Characteristics /Package Drawing

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Specification

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