Product Specification

RS3261 Wideband Bypass LNA

General Description

The RS3261 is a cascadable, wideband bypass LNA in a low-cost surface mount package. At 0.5 GHz, the amplifier provides 20 dB gain, +30 dBm OIP3 and 1 dB Noise Figure while drawing 30 mA current from a 3.3V supply.

The RS3261 provides excellent noise figure across a broad range of frequencies with the integration of a shut-down biasing capability to allow for operation for TDD applications. The low noise figure and high linearity performance allows the device to be used in both receiver and transmitter chains for high performance systems. The internal active bias circuit also enables stable operation over bias and temperature variations and can be biased from a single positive supply ranging from +3 to +5 volts. The amplifier is internally matched using a high-performance E-pHEMT process and is housed in a small 2x2 mm surface-mount package.

The RS3261 covers the 0.03 - 4 GHz frequency band and is targeted for land mobile radio or other applications requiring high linearity and/or low noise figure

Applications

- Land mobile radio
- Repeater/DAS
- General purpose RF
- TDD/FDD system

Features

- Wideband and Robust
  - 0.03 – 4 GHz operational frequency
- Outstanding performance in small package
  - 20 dB Gain
  - 29/34 dBm OIP3
  - 1 dB Noise Figure
  - Adjustable IDD via external resistor
  - 2 x 2 mm QFN package

Functional Diagram/Application Circuit

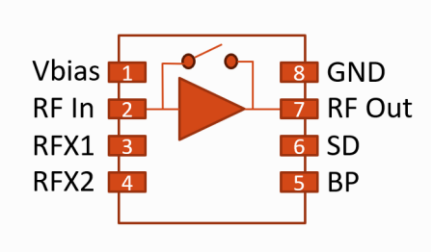


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
VDD to GND	-0.3	6	V
SD pin to GND	-0.3	6	V
Input Power		20	dBm
Maximum Junction Temperature		175	°C
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM (Per JESD22-A114)		TBD	
ESD Voltage – CDM (Per JESD22-C101)		TBD	

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Recommended Operating Conditions

Table 2

Parameter	Min	Typical	Max	Unit
Supply Voltage (All VDD)	3	3.3	5.25	V
Operating Temp Range	-40	25	105	°C
Control Logic High Voltage	1.17	3.3	5	V
Control Logic Low Voltage	0		0.63	V
Input Power			18	dBm

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

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LNA Mode Specification

Typical Application Circuit, VDD=3.3V, 30mA IDD, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 3

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4000	MHz
Gain	30-520MHz		21		dB
	520-1000MHz		20		
	1000-2000MHz		19		
	2000-4000MHz		16		
Input Return Loss	30-520MHz		-18		dB
	520-1000MHz		-15		
	1000-2000MHz		-15		
	2000-4000MHz		-10		
Output Return Loss	30-520MHz		-15		dB
	520-1000MHz		-20		
	1000-2000MHz		-18		
	2000-4000MHz		-12		
Output P1dB	3.3V, 30mA		16		dBm
Output IP3	3.3V, 30mA. Pout = +1 dBm/tone, Frequency Spacing = 1 MHz		27		dBm
Noise Figure	30-520MHz		1.1		dB
	520-1000MHz		1.1		
	1000-2000MHz		1.2		
	2000-4000MHz		1.5		
Device Current, IDD	LNA ON, Bypass OFF. 3.3V, Normal operation		30		mA
	LNA OFF, Bypass OFF. 3.3V, Normal operation		TBD		µA
	LNA OFF, Bypass ON. 3.3V, Normal operation		TBD		µA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			150		µA
Switching Time	LNA ON to OFF		0.5		µS
	LNA OFF to ON		8		µS
	LNA to Bypass		2		µS
	Bypass to LNA		5		µS
	Bypass to OFF, OFF to Bypass		2		µS

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Typical Application Circuit, VDD=5V, 60mA IDD, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 4

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4000	MHz
Gain	30-520MHz		21		dB
	520-1000MHz		20		
	1000-2000MHz		19		
	2000-4000MHz		16		
Input Return Loss	30-520MHz		-17		dB
	520-1000MHz		-16		
	1000-2000MHz		-18		
	2000-4000MHz		-10		
Output Return Loss	30-520MHz		-13		dB
	520-1000MHz		-18		
	1000-2000MHz		-18		
	2000-4000MHz		-16		
Output P1dB	5V, 60mA		19		dBm
Output IP3	5V, 60mA. Pout = +1 dBm/tone, Frequency Spacing = 1 MHz		33		dBm
Noise Figure	30-520MHz		1.1		dB
	520-1000MHz		1.1		
	1000-2000MHz		1.2		
	2000-4000MHz		1.5		
Device Current,IDD	LNA ON, Bypass OFF. 5V, Normal operation		60		mA
	LNA OFF, Bypass OFF. 5V, Normal operation		TBD		µA
	LNA OFF, Bypass ON. 5V, Normal operation		TBD		µA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			150		µA
Switching Time	LNA ON to OFF		0.5		µS
	LNA OFF to ON		8		µS
	LNA to Bypass		2		µS
	Bypass to LNA		5		µS
	Bypass to OFF, OFF to Bypass		2		µS

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Typical Application Circuit, VDD=3.3V, 15mA IDD, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 5

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4000	MHz
Gain	30-520MHz		18.5		dB
	520-1000MHz		18		
	1000-2000MHz		16.5		
	2000-4000MHz		13		
Input Return Loss	30-520MHz		-17		dB
	520-1000MHz		-14		
	1000-2000MHz		-12		
	2000-4000MHz		-8		
Output Return Loss	30-520MHz		-15		dB
	520-1000MHz		-20		
	1000-2000MHz		-18		
	2000-4000MHz		-12		
Output P1dB	3.3V, 15mA		16		dBm
Output IP3	3.3V, 15mA. Pout = +2 dBm/tone, Frequency Spacing = 1 MHz		27		dBm
Noise Figure	30-520MHz		1.5		dB
	520-1000MHz		1.5		
	1000-2000MHz		1.6		
	2000-4000MHz		1.8		
Device Current, IDD	LNA ON, Bypass OFF. 3.3V, Normal operation		15		mA
	LNA OFF, Bypass OFF. 3.3V, Normal operation		TBD		µA
	LNA OFF, Bypass ON. 3.3V, Normal operation		TBD		µA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			150		µA
Switching Time	LNA ON to OFF		0.5		µS
	LNA OFF to ON		8		µS
	LNA to Bypass		2		µS
	Bypass to LNA		5		µS
	Bypass to OFF, OFF to Bypass		2		µS

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Bypass Mode Specification

Typical Application Circuit, VDD=3.3V, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 6

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4000	MHz
Insertion Loss	30-520MHz		-0.6		dB
	520-1000MHz		-0.7		
	1000-2000MHz		-1.2		
	2000-4000MHz		-1.7		
Input Return Loss	30-520MHz		-18		dB
	520-1000MHz		-15		
	1000-2000MHz		-13		
	2000-4000MHz		-10		
Output Return Loss	30-520MHz		-18		dB
	520-1000MHz		-15		
	1000-2000MHz		-13		
	2000-4000MHz		-10		
Output P1dB	3.3V, 30-4000MHz		21		dBm
Output IP3	3.3V, Pin = +1 dBm/tone, Frequency Spacing = 1 MHz		38		dBm
Device Current, IDD	LNA OFF, Bypass ON. 3.3V, Normal operation		500		µA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			30		µA
Thermal Resistance, θ_{jc}	Junction to case		TBD		°C/W

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Typical Application Circuit, VDD=5V, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 7

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		4000	MHz
Insertion Loss	30-520MHz		-0.6		dB
	520-1000MHz		-0.8		
	1000-2000MHz		-1.2		
	2000-4000MHz		-1.6		
Input Return Loss	30-520MHz		-18		dB
	520-1000MHz		-15		
	1000-2000MHz		-13		
	2000-4000MHz		-10		
Output Return Loss	30-520MHz		-18		dB
	520-1000MHz		-15		
	1000-2000MHz		-13		
	2000-4000MHz		-10		
Output P1dB	5V, 30-4000MHz		21		dBm
Output IP3	5V, Pin = +1 dBm/tone, Frequency Spacing = 1 MHz		38		dBm
Device Current, IDD	LNA OFF, Bypass ON. 5V, Normal operation		600		μA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			30		μA
Thermal Resistance, θ_{jc}	Junction to case		TBD		°C/W

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Pin Diagram

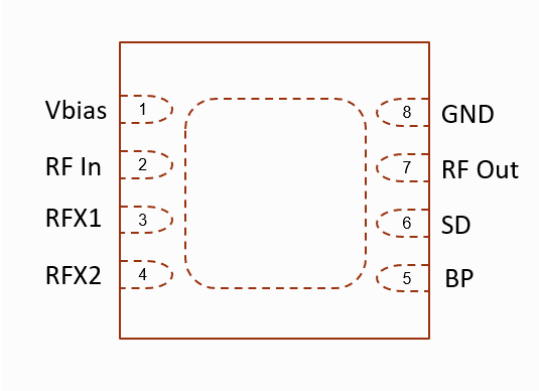


Figure 2

Pin Description

Table 8

Pad No.	Label	Description
1	Vbias	Bias voltage. Bias input voltage for reference, and internal control circuits
2	RF In	RF Input.
3	RFX1	Interstage RF connection. For high frequency application, a capacitor must be placed as close as possible to this pin
4	RFX2	Interstage RF connection. For high frequency application, a capacitor must be placed as close as possible to this pin
5	BP	Bypass control input.
6	SD	Shutdown Input.
7	RF Out	RF Output.
8	GND	Ground pin.

Control Logic

Table 9

Mode	SD Pin 6 logic	BP Pin 5 logic
Amplifier Enable	0	0
Bypass	0	1
Isolation, amplifier disable, bypass disable	1	0
Bypass	1	1

Application Circuit

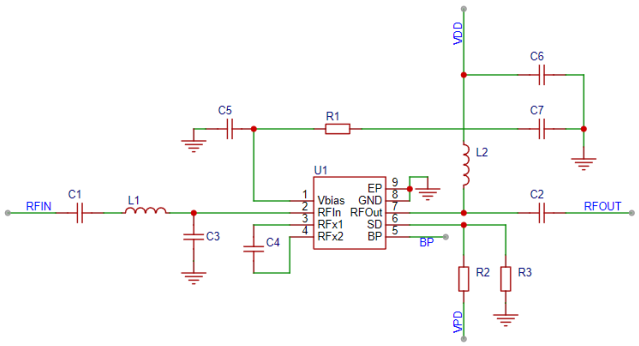


Figure 3

Table 10

Reference Designator	Value	Description
C5 、C6	10nF	0402
C1、C2、C4	1nF	0402
C7	100pF	0402
C3	0.5pF	0402(For below 2GHz application, it's ok to NC)
R1	Rbias	0402(5V 60mA, use 1.2kohm)
R3	NC	0402
R2	0ohm	0402
L2	0.9uH	0402
L1	0.7nH	0201(For below 2GHz application, it's ok to NC)

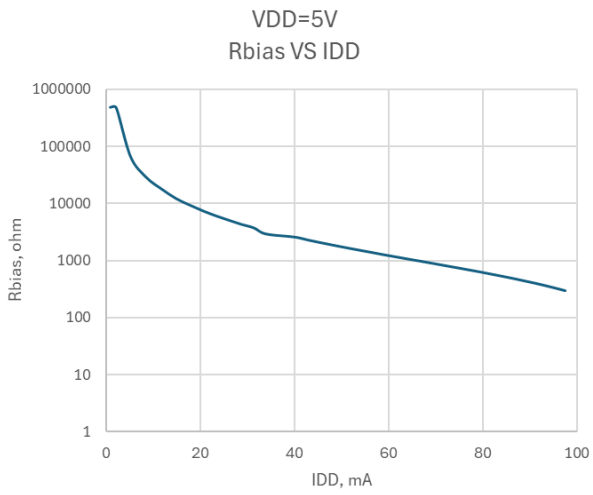


Figure 4

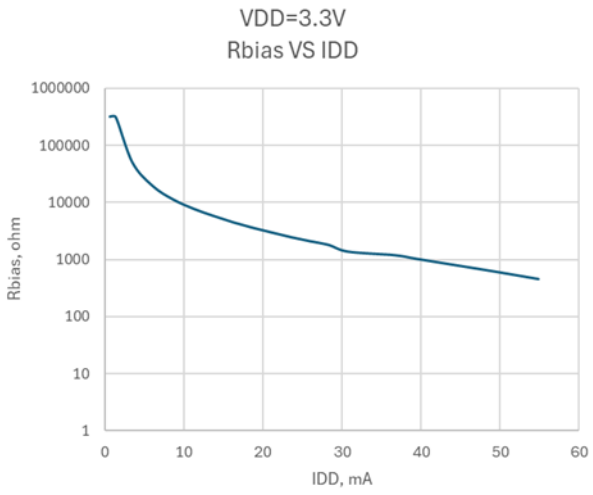


Figure 5

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Typical Performance Characteristics(3.3V 30mA)

Figure 6. Gain

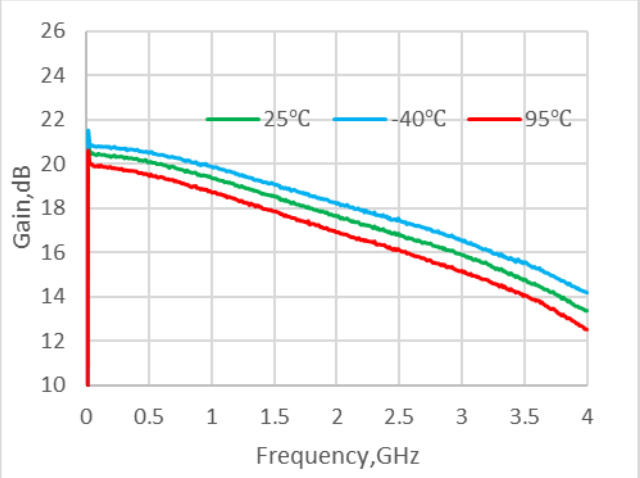


Figure 7. Input Return Loss

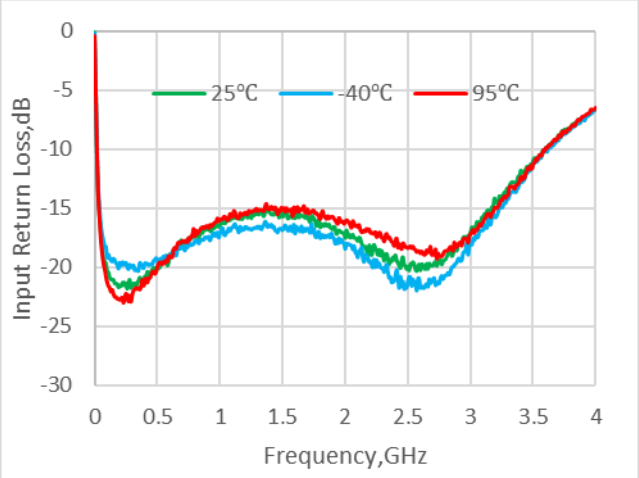


Figure 8. Output Return Loss

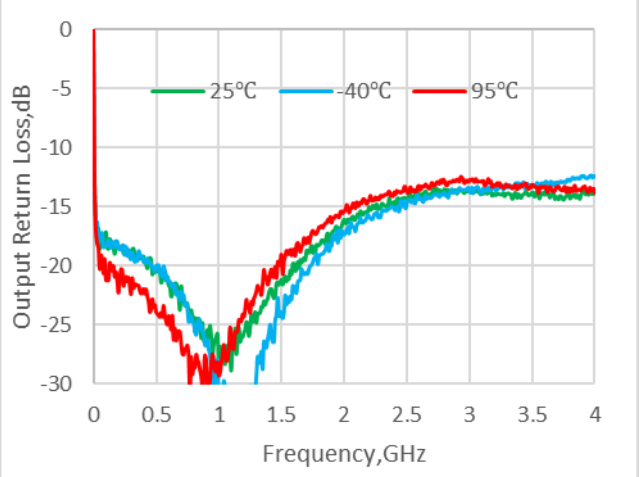


Figure 9. Noise Figure

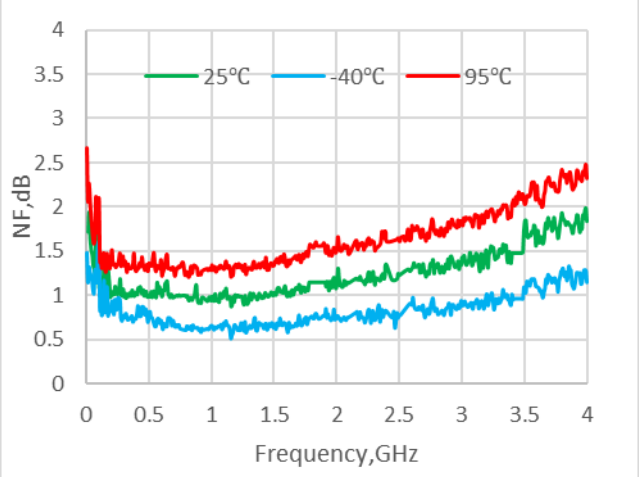


Figure 10. P1dB

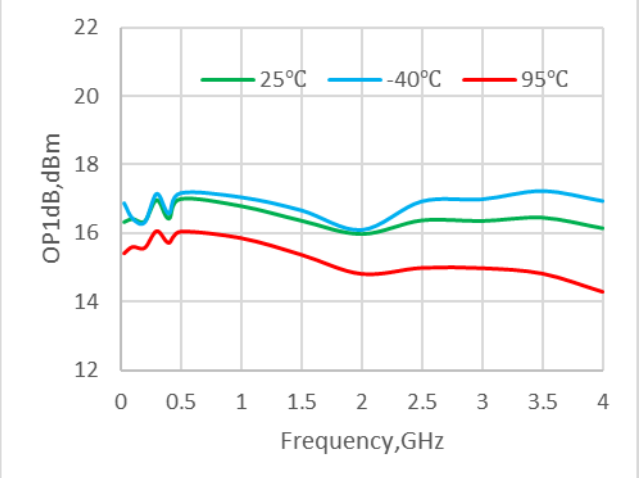
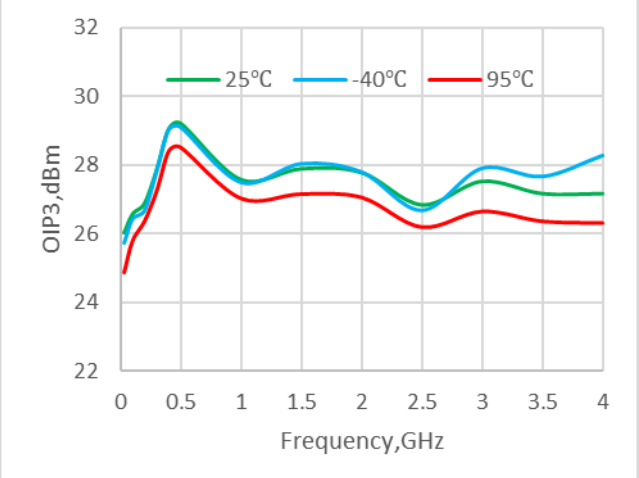


Figure 11. OIP3



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Typical Performance Characteristics(3.3V 15mA)

Figure 12. Gain

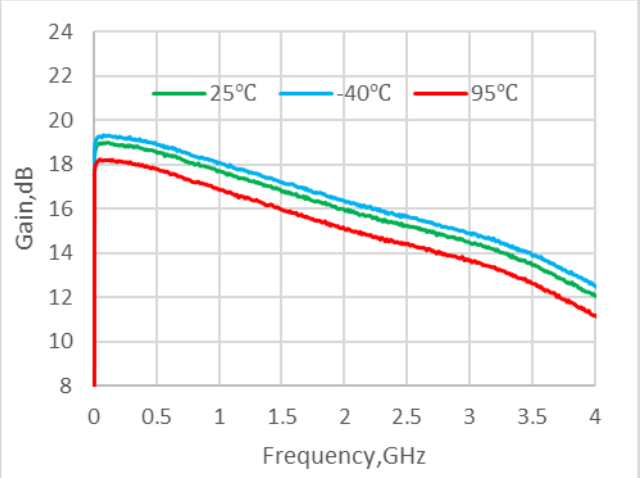


Figure 13. Input Return Loss

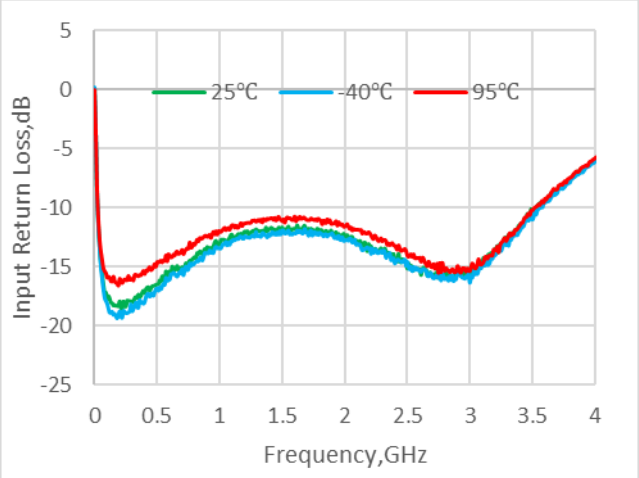


Figure 14. Output Return Loss

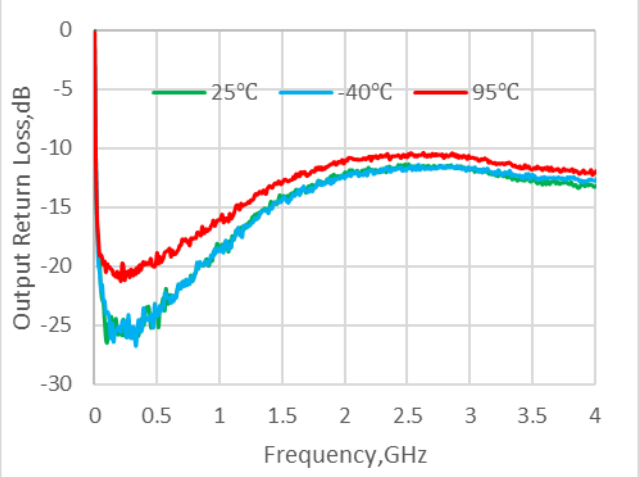


Figure 15. Noise Figure

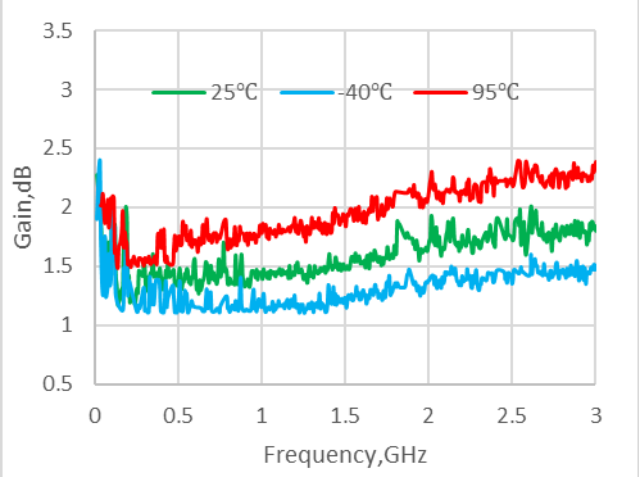


Figure 16. P1dB

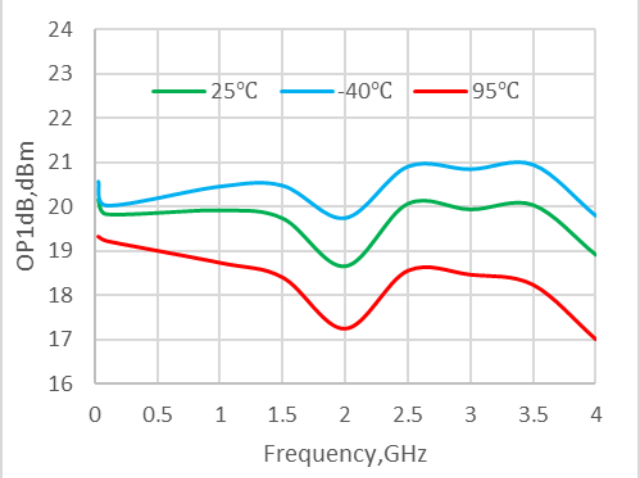
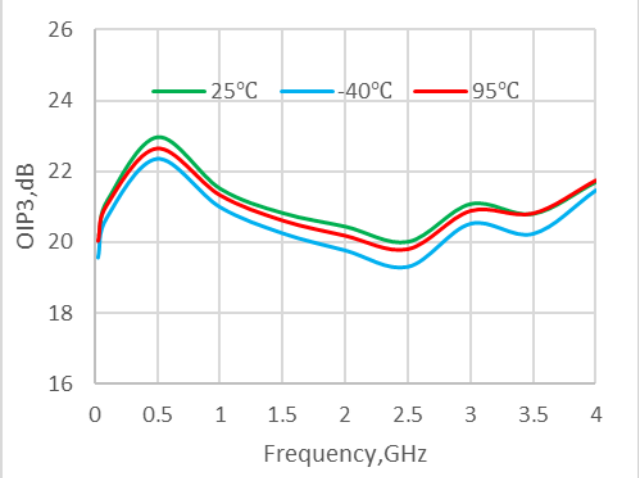


Figure 17. OIP3



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Typical Performance Characteristics(5V 60mA)

Figure 18. Gain

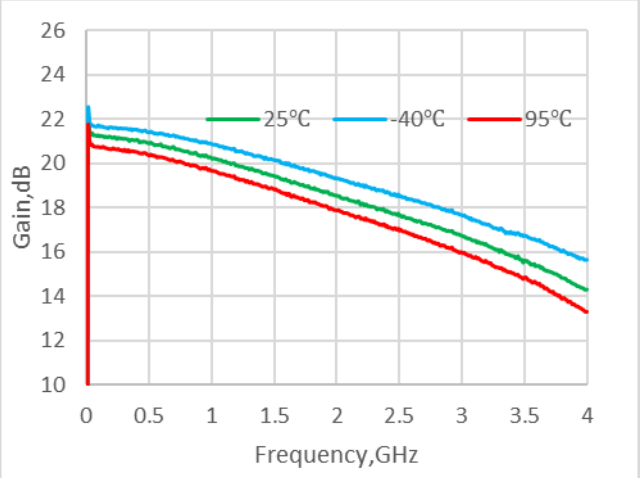


Figure 19. Input Return Loss

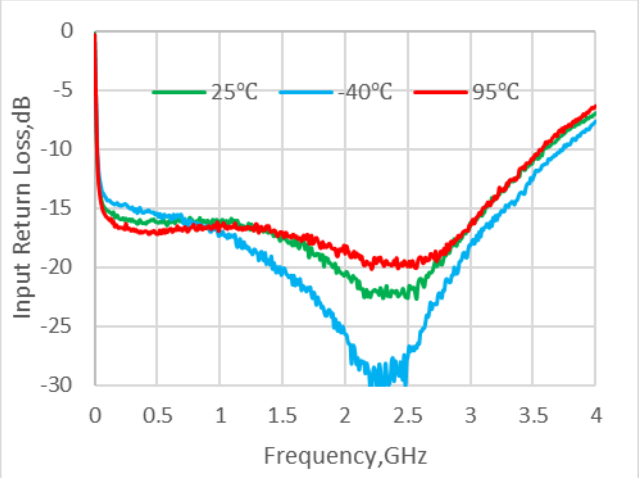


Figure 20. Output Return Loss

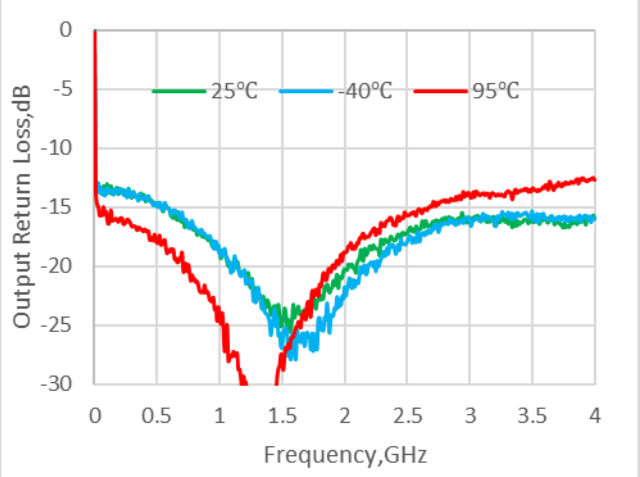


Figure 21. Noise Figure

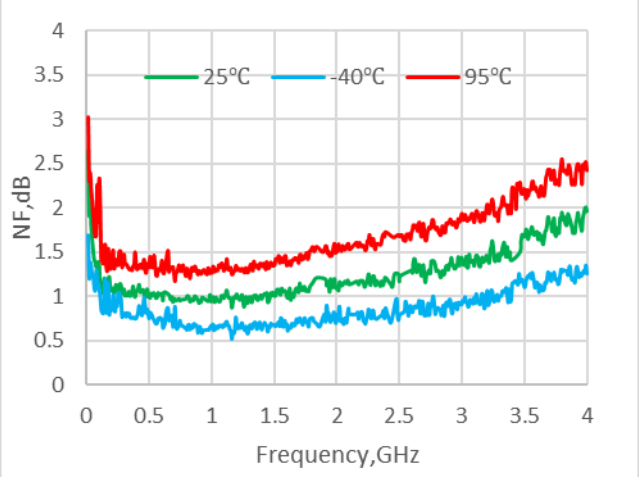


Figure 22. P1dB

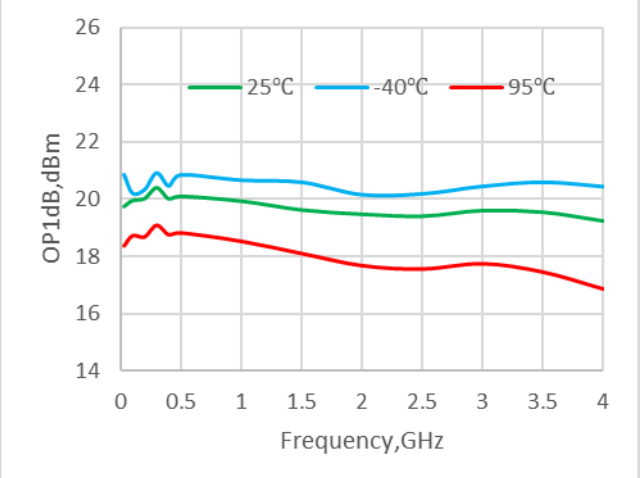
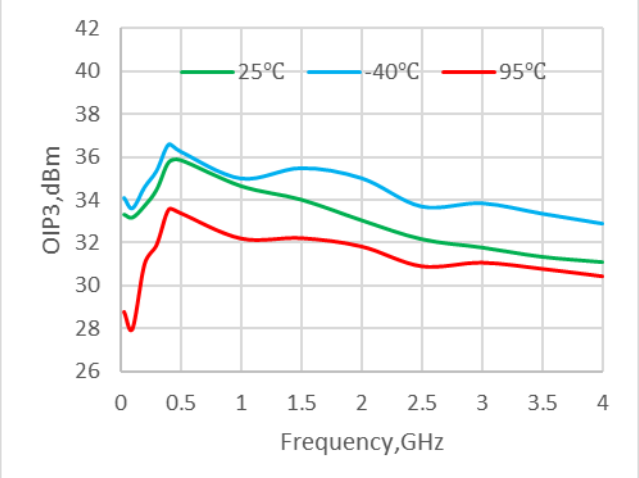


Figure 23. OIP3



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Typical Performance Characteristics(Bypass mode 3.3V)

Figure 24. Insertion Loss

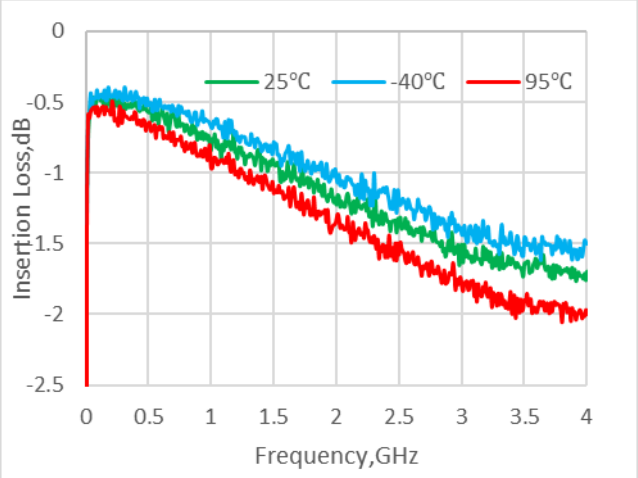


Figure 25. Input Return Loss

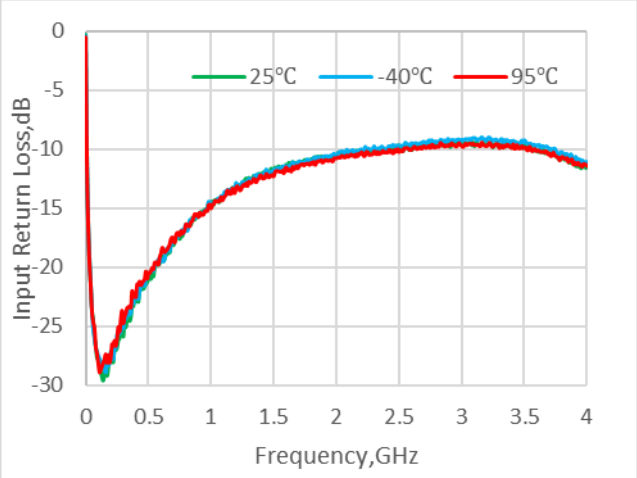


Figure 26. Output Return Loss

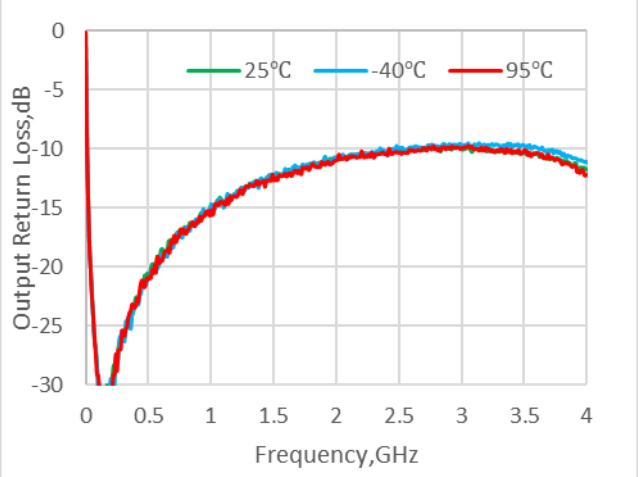


Figure 27. OIP3

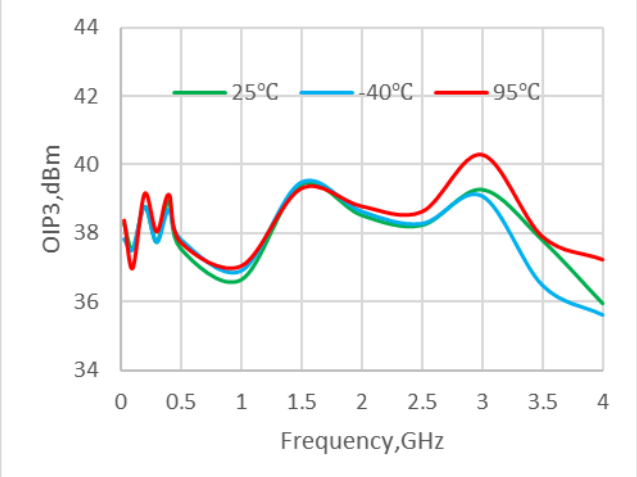
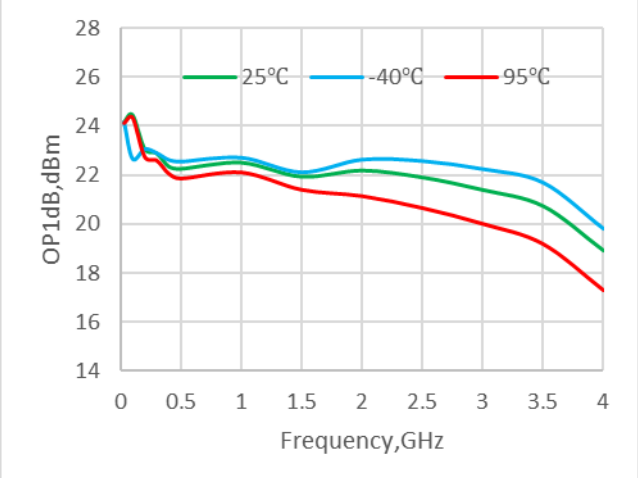


Figure 28. P1dB



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Typical Performance Characteristics(Bypass mode 5V)

Figure 29. Insertion Loss

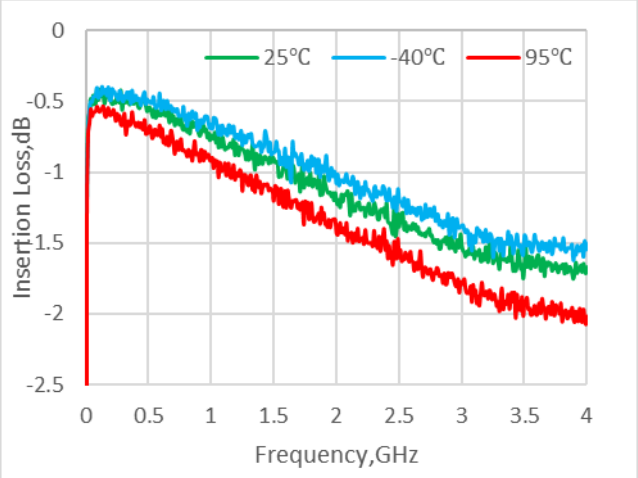


Figure 30. Input Return Loss

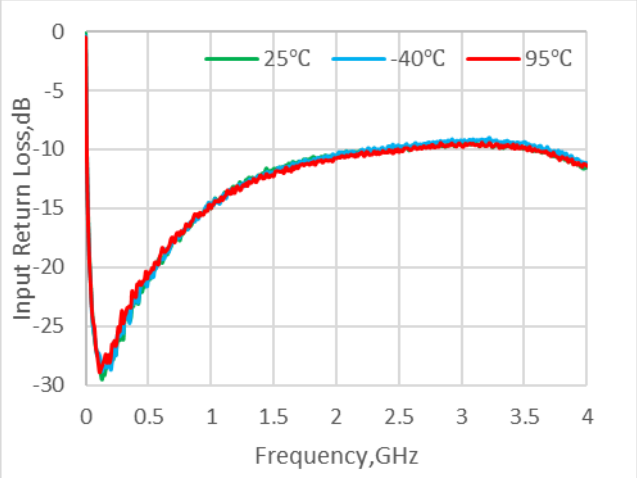


Figure 31. Output Return Loss

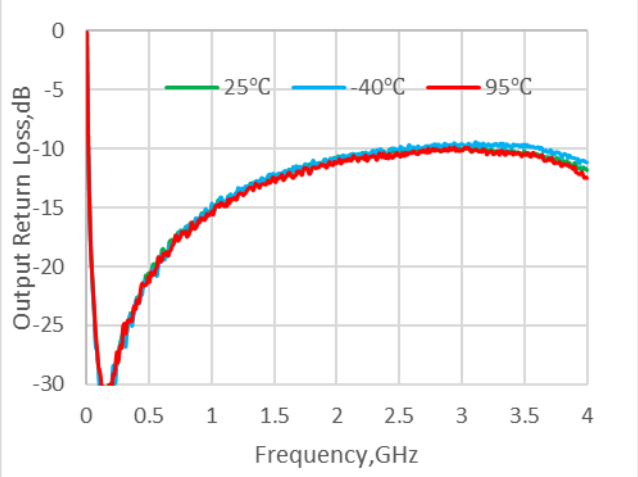


Figure 32. OIP3

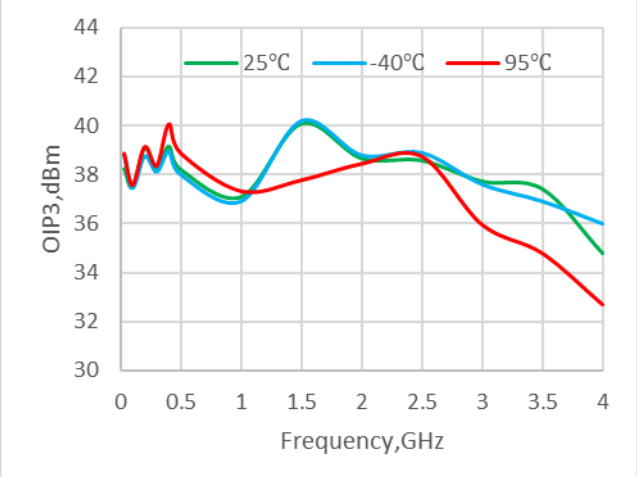
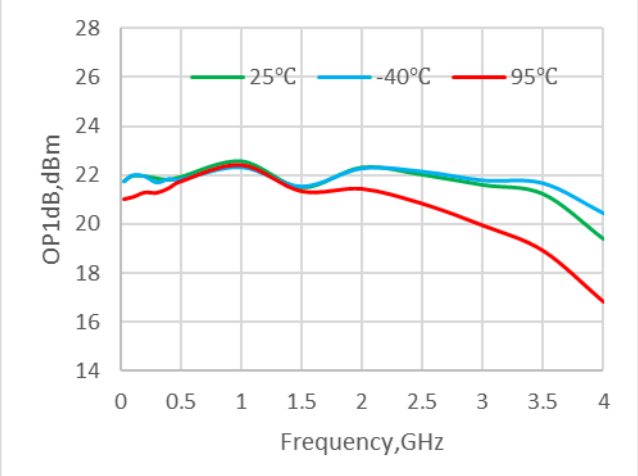
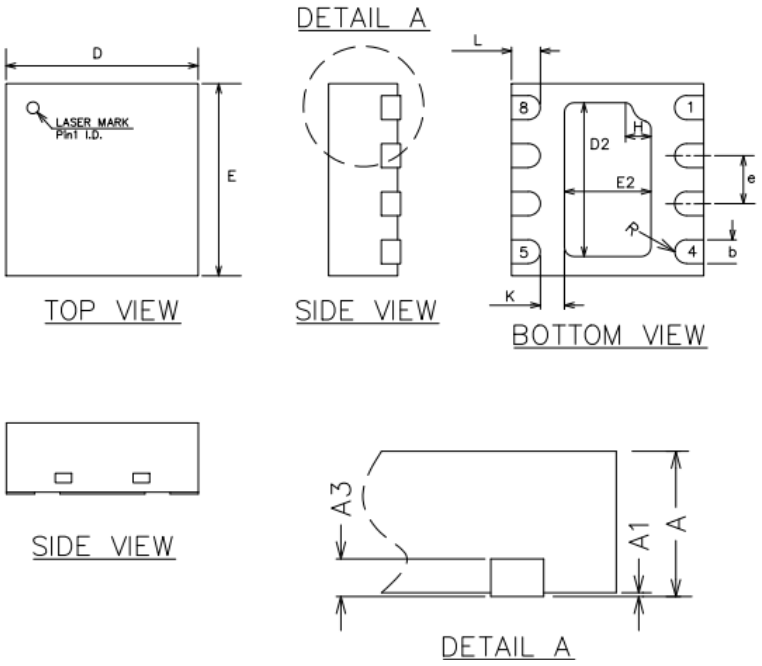


Figure 33. P1dB



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Package Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	1.50	1.60	1.70
E2	0.80	0.90	1.00
e	0.45	0.50	0.55
H		0.27REF	
K	0.20	–	–
L	0.20	0.30	0.40
R	0.13	–	–

Figure 34

Revision History

Table 5

Revision Number	Revision Date	Description	Modifications
0.2		Draft	—
0.4	2024/10/11	Update ES Data	
0.5	2024/10/23	Update schematic and switching time	
0.6	2025/05/28	Update General Description/Features/Specification/Pin Diagram/Typical Performance Characteristics/Application Circuit/Package Drawing	
0.7	2025/10/13	Update3.3v/15mA Typical Performance Characteristics	

Document Categories

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The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

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