Product Specification

RS3192X Wideband Flat LNA

General Description

The RS3192X is a cascadable, wideband LNA in a low-cost surface mount package. At 2.6 GHz, the amplifier provides ＞20 dB gain, +32 dBm OIP3 and 0.6 dB Noise Figure.

The RS3192X provides with the integration of a shut-down biasing capability to allow for operation for TDD applications. The low noise figure and high linearity performance allows the device to be used in both receiver and transmitter chains for high performance systems. The internal active bias circuit also enables stable operation over bias and temperature variations and can be biased from a single positive supply ranging from +2.7 to +5.5 volts. The amplifier is internally matched using GaAs-pHEMT process and is housed in a small 2 x 2 mm surface-mount package.

The RS3192X covers the 0.5 – 5 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure

Applications

- 5G massive MIMO
- 2G/3G/4G mobile infrastructure
- Repeater/DAS
- General purpose RF
- TDD/FDD system

Features

- Wideband
  - 0.6 – 5 GHz operational frequency
- Balanced performance in small package
  - ＞20 dB Gain @ 2.6 GHz
  - 0.6 dB Noise Figure @ 2.7 GHz
  - 2 x 2mm QFN8L package
- ESD protection on all pins CLASS 1B

Functional Diagram/Application Circuit

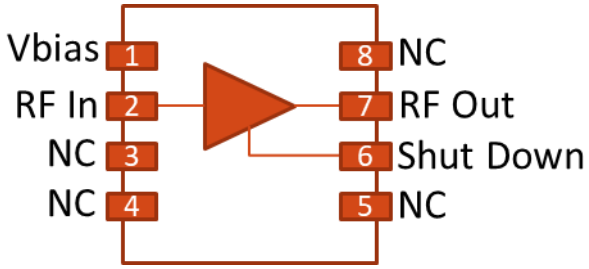


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
VDD to GND		7	V
SD pin to GND		7	V
Input Power, cw signal		23	dBm
Maximum Junction Temperature		175	°C
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM		Class 1B	
ESD Voltage – CDM		Class C1	

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Recommended Operating Conditions

Table 2

Parameter	Min	Typical	Max	Unit
Supply Voltage (All VDD)	2.7	5	5.5	V
Operating Temp Range	-40	25	105	°C
Control Logic High Voltage	1.2		VDD	V
Control Logic Low Voltage	0		0.6	V
Input Power, cw signal			20	dBm

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

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Specification

Typical Application Circuit, VDD=5V, T_C = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 3

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		5000	MHz
Gain	Fre@1GHz		22		dB
	Fre@2GHz		21		dB
	Fre@2.5GHz		21		dB
	Fre@3GHz		22		dB
	Fre@3.5GHz		23		dB
	Fre@5GHz		18		dB
Input Return Loss			-12		dB
Output Return Loss			-20		dB
Passband Ripple	ΔfRF=100MHz		0.5	1.2	dB
Reverse Isolation	Fre@0.6~4.2GHz		-31	-20	dB
	Fre@4.2~5GHz		-20	-15	dB
Output P1dB	Fre@3.5GHz		17		dBm
Output IP3	Pout@+5dBm/tone, Δf@1MHz		32.5		dBm
Noise Figure	evaluation board trace loss excluded		0.6		dB
Device Current, IDD	ON, Normal operation, VSD @ 0 V		65	80	mA
	OFF, VSD @ 3.3 V		3.0		mA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Device ON or OFF Timing	50% of VPD to 90% or 10% RF Output		60	500	nS
Thermal Resistance, θ_{jc}	Junction to case		42		°C/W

Pin Diagram

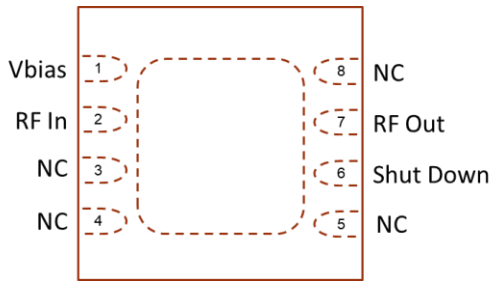


Figure 2

Pin Description

Table 4

Pad No.	Label	Description
1	Vbias	Bias voltage. Bias input voltage for reference, and internal control circuits
2	RF In	RF Input. Requires a DC-blocking capacitor and an inductor.
3,4,5,8	NC	No connection. Recommend to connect to the PCB ground plane.
6	Shut Down	Shutdown Input. A logic-high disables the device.
7	RF Out	RF Output. RFOUT is internally matched to 50Ω and incorporates an internal DC-blocking capacitor.

Control Logic

Table 5

Mode	SD Pin 6 logic
Amplifier Enable	0
Amplifier Shunt down	1

Typical Performance Characteristics

Figure 3. Gain

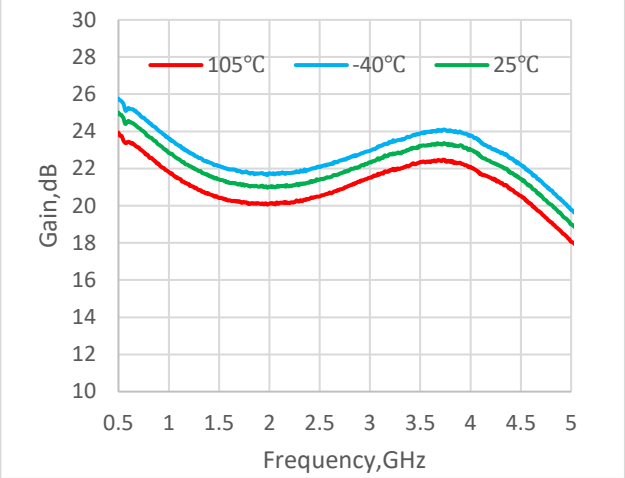


Figure 4. Input Return Loss

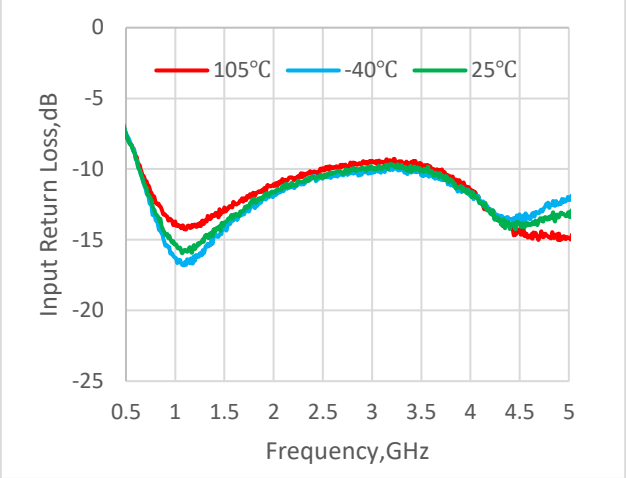


Figure 5. Output Return Loss

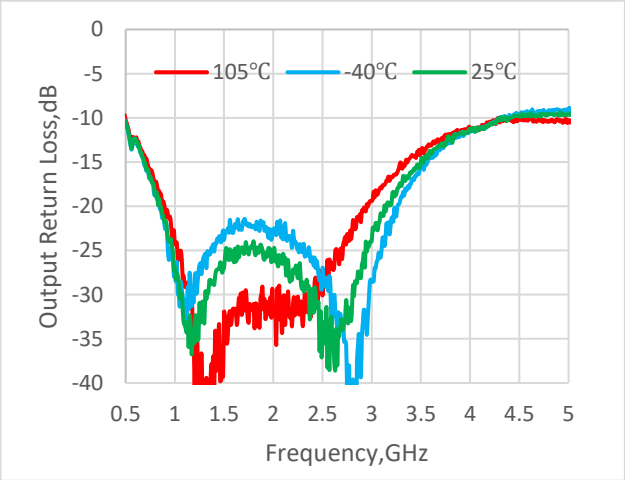


Figure 6. Noise Figure

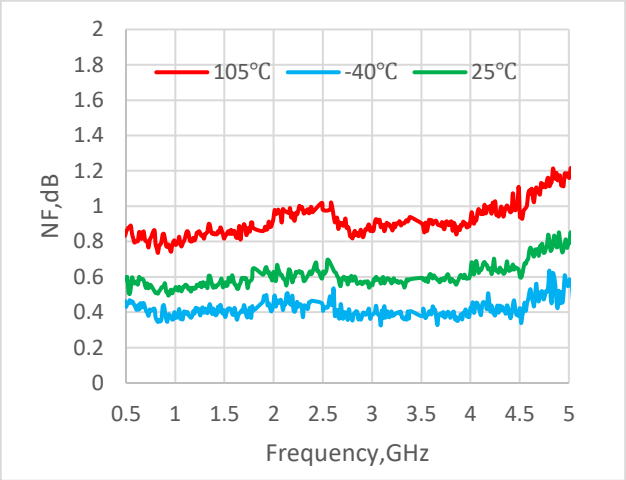


Figure 7. P1dB

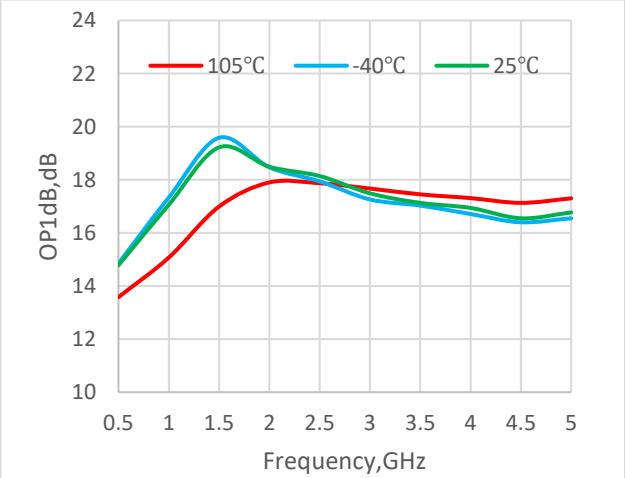
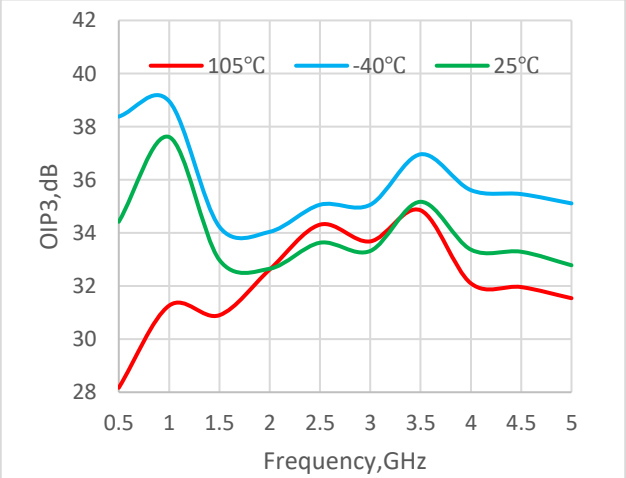


Figure 8. OIP3



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Application Circuit

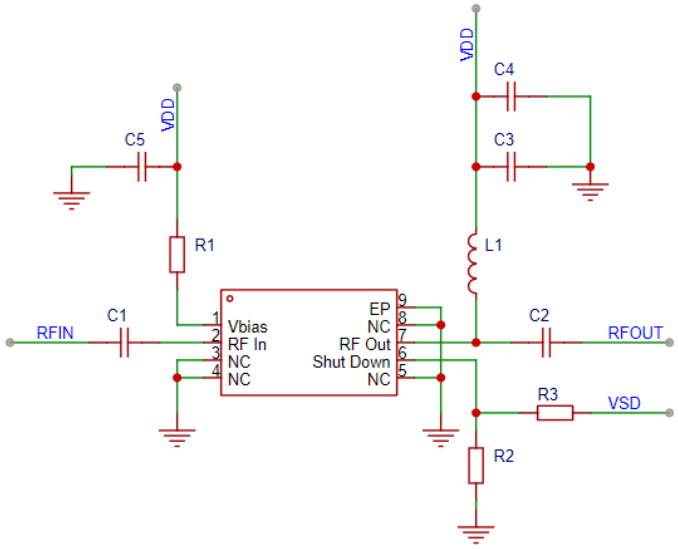


Figure 9

Table 6

Reference Designator	Value	Description
C1、C2、C5	100pF	0402
C3	1uF	0402
C4	10nF	0402
R1	3.3K	0402
R2	20K	0402
R3	0Ω	0402
L1	20nH	0402

Figure 10. Rbias VS Idd@5V-Vdd

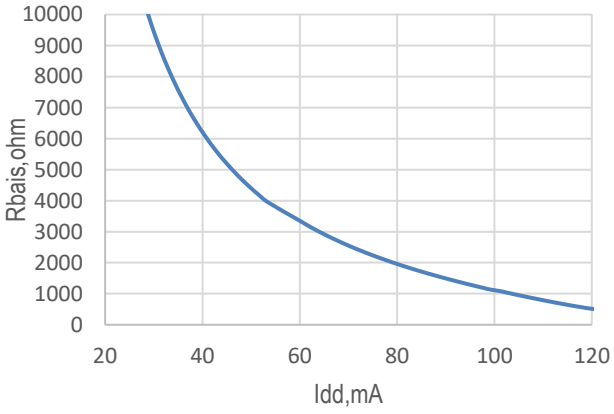
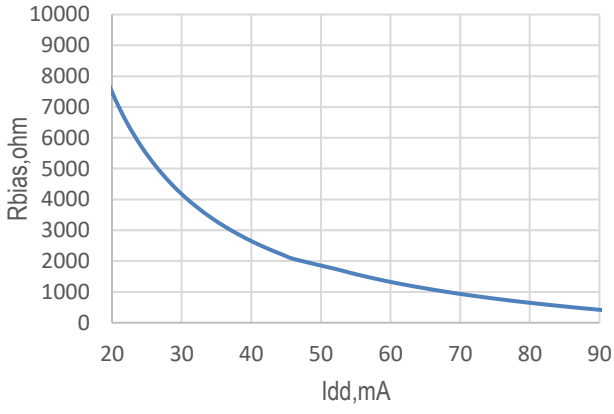
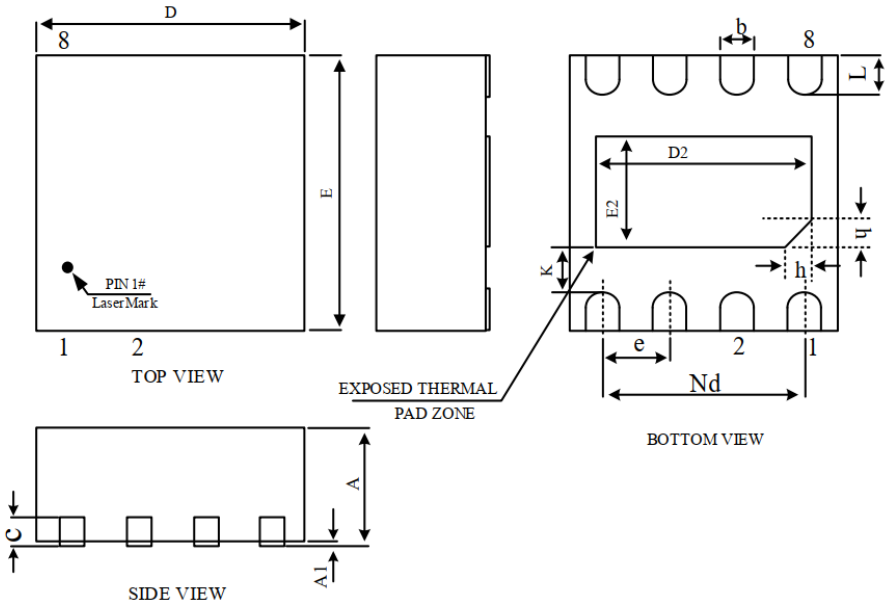


Figure 11. Rbias VS Idd@3.3V-Vdd



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Package Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
Nd		1.50BSC	
e		0.50BSC	
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h		0.20REF	

Figure 12

Revision History

Table 7

Revision Number	Revision Date	Description	Modifications
0	2020/11/7	Draft	—
0.1	2020/12/8	Initial release	
0.2	2021/9/7		Update App circuit ,plots and data
0.3	2022/1/6	Released	
1.0	2022/2/16		
1.1	2022/3/28	Update	Modify Figure
1.2	2022/5/28	Update	Update Information
1.3	2023/5/12	Update	Add Idd @ VPD=3.3V
1.4	2025/5/16	Update	General Description/Features/Specification/Pin Diagram/Typical Performance Characteristics/Application Circuit/Package Drawing

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Specification

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