Product Specification

RS3113 15dB Gain High Input P1dB Wideband Flat Gain Block

General Description

The RS3113 is a cascadable, wideband gain block amplifier in a low-cost surface mount package. At 3.5 GHz, the amplifier provides 15 dB gain, +33 dBm OIP3 and 1.7 dB Noise Figure while drawing 65 mA current from a 5V supply.

The RS3113 provides very flat gain across a broad range of frequencies with the integration of a shut-down biasing capability to allow for operation for TDD applications. The low noise figure and high linearity performance allows the device to be used in both receiver and transmitter chains for high performance systems. The internal active bias circuit also enables stable operation over bias and temperature variations and can be biased from a single positive supply ranging from +3.3 to +5 volts. The amplifier is internally matched using a high-performance E-pHEMT process and is housed in a small 2x2 mm surface-mount package.

The RS3113 covers the 0.03 – 3 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure

Applications

- 5G massive MIMO
- 2G/3G/4G mobile infrastructure
- Repeater/DAS
- General purpose RF
- TDD/FDD system

Features

- Wideband
  - 0.03 – 3 GHz operational frequency
  - Flat gain, over 0.03 – 3 GHz, gain variation 1 dB
- Balanced performance in small package
  - 15 dB Gain @ 3 GHz
  - 33 dBm OIP3 @ 3 GHz
  - 20 dBm OP1dB @ 3 GHz
  - 65mA current consumption under 5V
  - 2 x 2mm QFN package
- ESD protection on all pins (HBM > 1000V)

Functional Diagram/Application Circuit

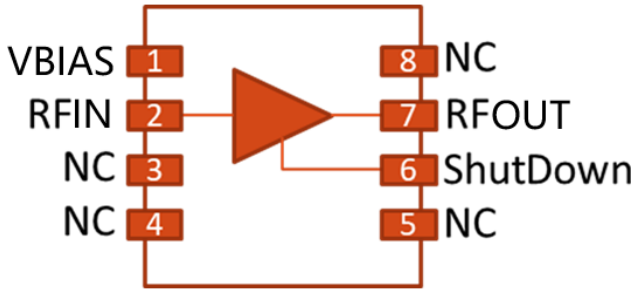


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
VDD to GND	-0.3	6	V
ShutDown pin to GND	-0.3	6	V
Input Power, CW signal		20	dBm
Maximum Junction Temperature		175	°C
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM (Per JESD22-A114)		Class 1B	

Exceeding any of these listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Recommended Operating Conditions

Table 2

Parameter	Min	Typical	Max	Unit
Supply Voltage (All VDD)	4.75	5	5.25	V
Operating Temp Range	-40	25	105	°C
Control Logic High Voltage	1.4	3.3	5	V
Control Logic Low Voltage	0		0.63	V
Input Power, CW signal			19	dBm

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

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Specification

Typical Application Circuit, VDD=5V, TC = +25°C, PCB board trace and connector losses are de-embedded unless otherwise noted.
Table 3

Parameters	Conditions	Min	Typ	Max	Units
Operational Frequency Range		30		3000	MHz
Gain	30-3000MHz		15		dB
Input Return Loss	30-3000MHz		-15		dB
Output Return Loss	30-3000MHz		-20		dB
Output P1dB			20		dBm
Output IP3	Pout = +1 dBm/tone, Δf = 1 MHz		33		dBm
Noise Figure	Evaluation Board trace loss excluded		1.7		dB
Device Current, IDD	ON, Normal operation, VSD = 0 V		65		mA
OFF, Shut Down, VSD = 1.8 V			3		mA
Device Control Voltage, VSD	ON, Logic Low	0	0.63		V
OFF, Logic High		1.17		VDD	V
Control Pin Current, ISD			150		µA
Device ON or OFF Timing	50% of VSD to 90% or 10% RF Output		1		µS
Thermal Resistance, θjc	Junction to case		TBD		°C/W

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Pin Diagram

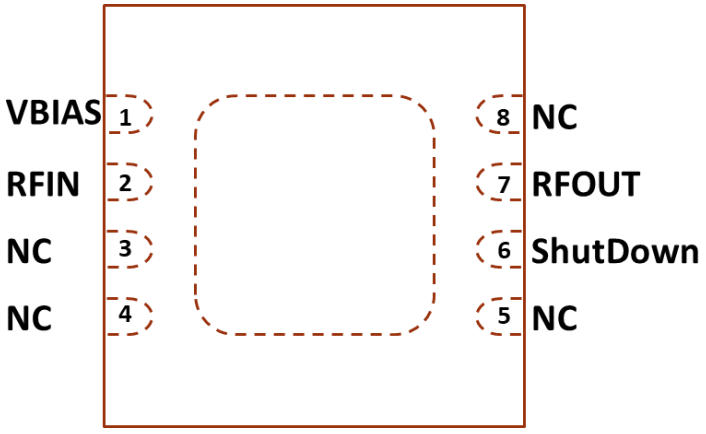


Figure 2

Pin Description

Table 4

Pad No.	Label	Description
1	VBIAS	Bias voltage. Bias input voltage for reference, and internal control circuits
2	RFIN	RF Input. Requires a DC-blocking capacitor and an inductor.
3,4,5,8	NC	No connection. Recommend to connect to the PCB ground plane.
6	ShutDown	Shutdown Input. A logic-high disables the device.
7	RFOUT	RF Output. RFOUT is internally matched to 50Ω and incorporates an internal DC-blocking capacitor.

Control Logic

Table 5

Mode	ShutDown Pin 5 logic
Amplifier Enable	0
Amplifier Shutdown	1

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Application Information (Match from 30MHz to 3GHz)

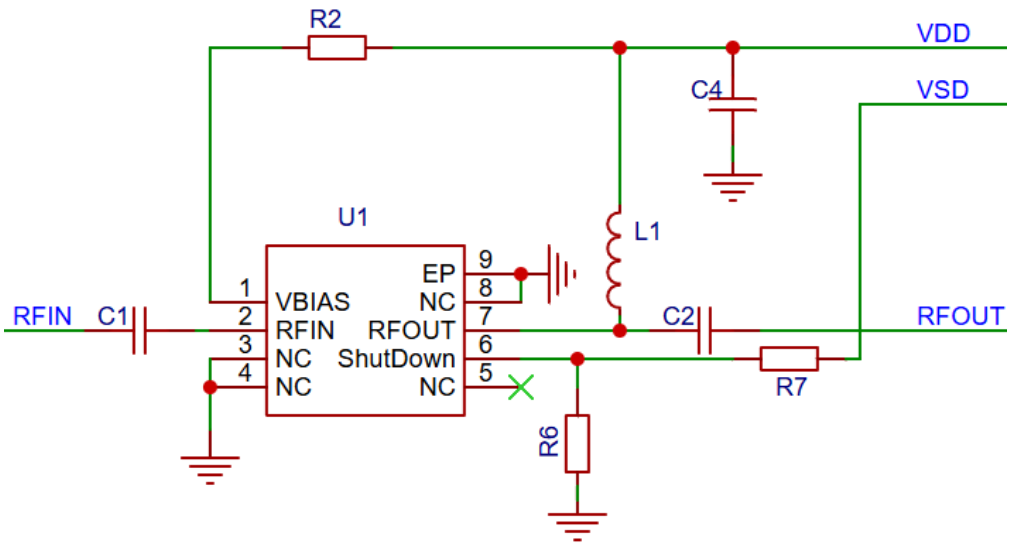


Figure 3

Table 6

Item	Quantity	Reference	Part	Footprint
1	2	C1,C2	1nF	0402
2	1	C4	100nF	0402
3	1	L1	390nH	0402
4	1	R7	0ohm	0402
5	1	R6	220K ohm	0402
6	1	R2	270 ohm	0402
7	1	U1	RS3113	

IDD VS Rbias

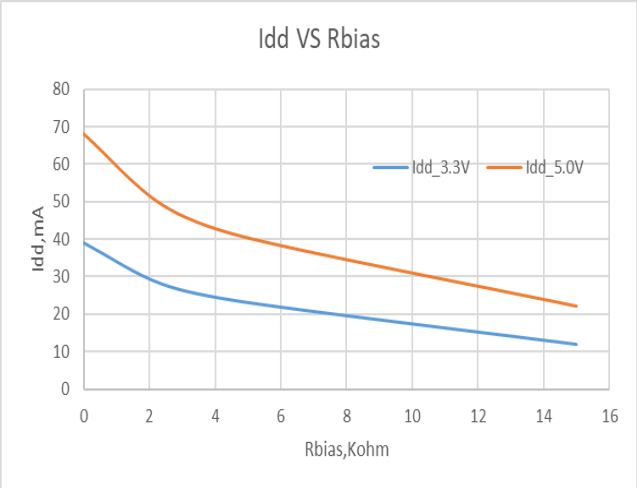


Figure 4

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Typical Performance Characteristics

Figure 5. Gain

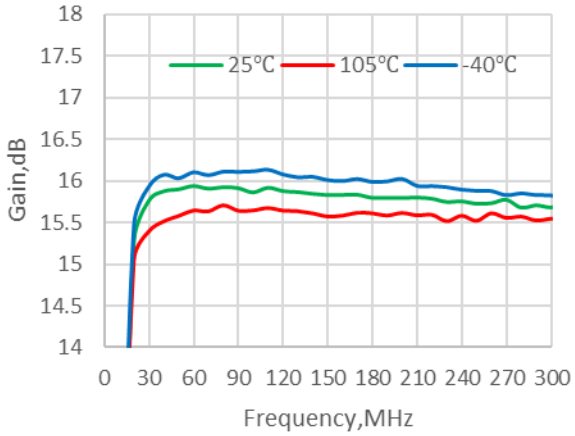


Figure 6. Gain

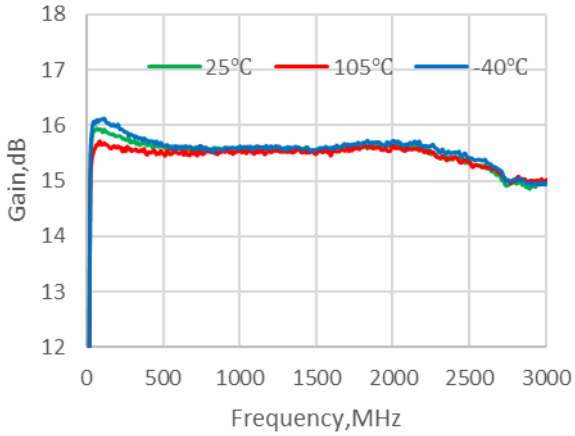


Figure 7. Input Return Loss

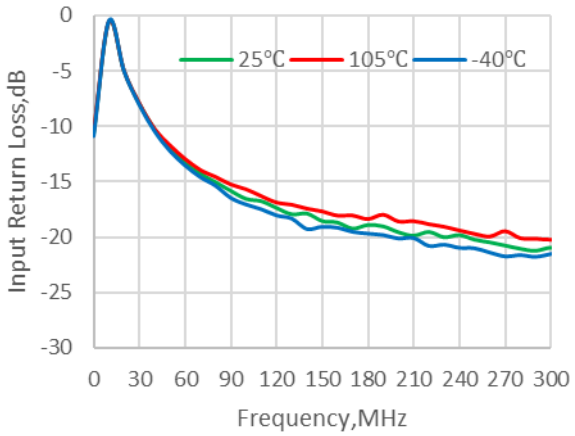


Figure 8. Input Return Loss

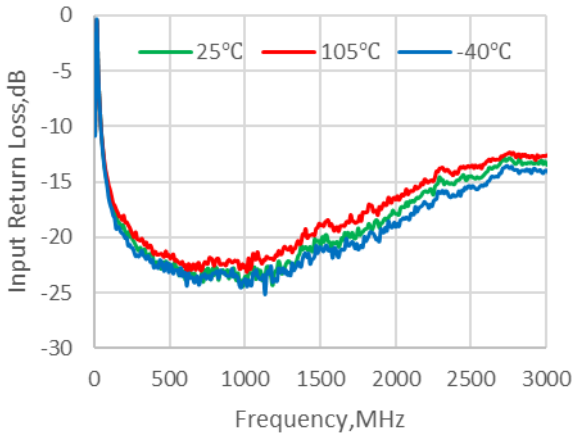


Figure 9. Output Return Loss

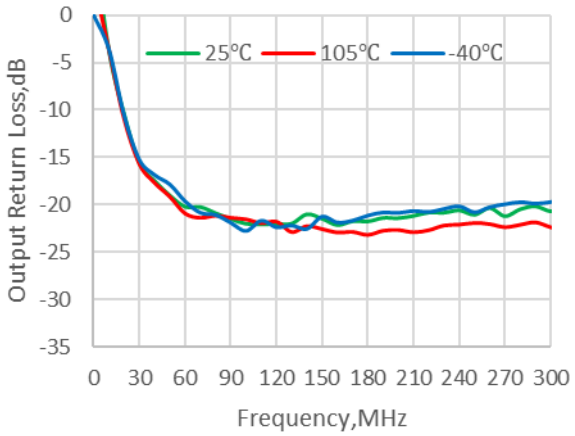
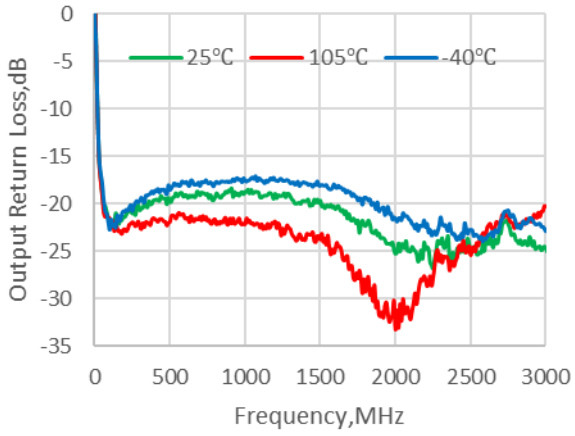


Figure 10. Output Return Loss



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Typical Performance Characteristics

Figure 11. Noise Figure

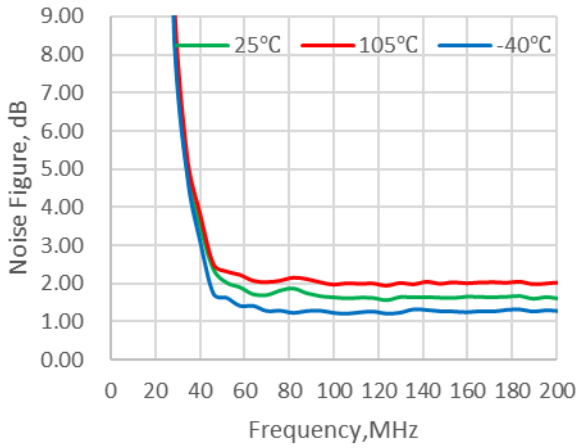


Figure12. Noise Figure

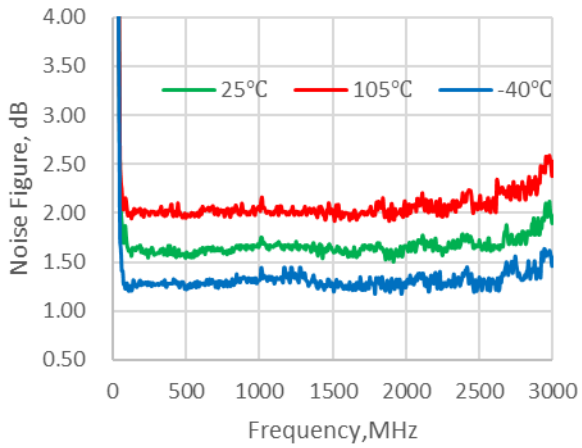


Figure13. OIP3

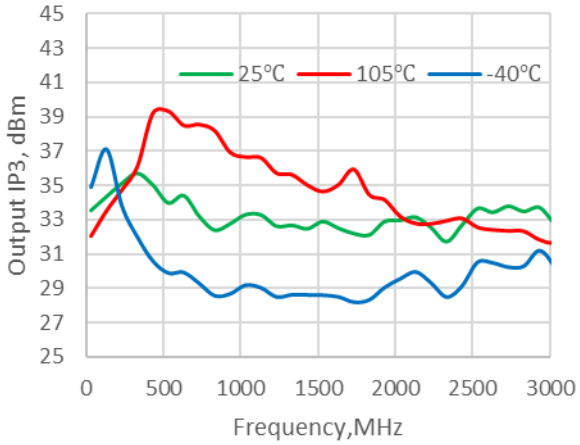
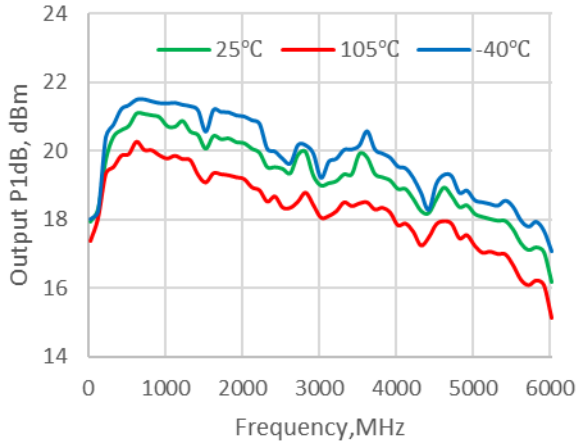
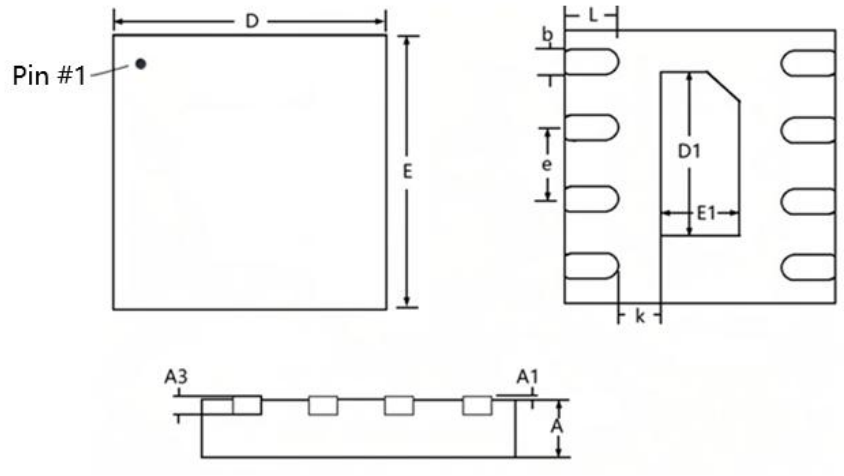


Figure 14. P1dB



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Package Drawing



Unit: mm			
Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00		0.05
A3	0.195	0.203	0.211
D	1.95	2.00	2.05
E	1.95	2.00	2.05
D1	1.15	1.20	1.25
E1	0.65	0.70	0.75
b	0.20	0.25	0.30
k	0.25MIN		
e	0.5TYP		
L	0.25	0.30	0.35

Figure 15

Revision History

Table 7

Revision Number	Revision Date	Description	Modifications
0	2020/11/7	Draft	—
0.1	2020/12/8	Initial release	
0.2	2021/9/3		Update App circuit ,plots and data
0.3	2023/5/19	Preliminary specification	Add application circuit
0.4	2023/6/17		Update noise figure
0.5	2024/4/26		Update max input power, ESD
0.6	2024/12/2		Update Idd VS Rbias
0.7	2025/5/23		Update curves,circuit,data

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Specification

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