Preliminary Specification

RS15512 Digital Step Attenuator

General Description

The RS15512 is a 6-bit digital step attenuator (DSA). It is available in a 4 mm × 4 mm, 24-lead QFN and provides 31.5dB attenuation range in 0.5dB and 1dB steps from 10 MHz to 4 GHz.

The RS15512 incorporates a negative voltage generator to operate with a single positive supply voltage from 2.7 V to 5.5 V applied to the VDD pin when all the GND pins are all connected to ground. The RS15512 provides both serial and parallel digital control interface.

Applications

- 3G/4G/5G wireless infrastructure
- Test equipment
- Land mobile radio system
- Point to point communication system

Features

- **Excellent RF Performance**
  - Flexible attenuation steps of 0.5dB and 1dB up to 31.5dB
  - High Attenuation Accuracy and Low Insertion Loss
- **High input linearity**
  - P0.1dB: 30 dBm typical
  - Third-order intercept (IP3): 50 dBm typical
- **Programming interface**
  - Direct parallel
  - Latched parallel
  - Serial

Functional Block Diagram

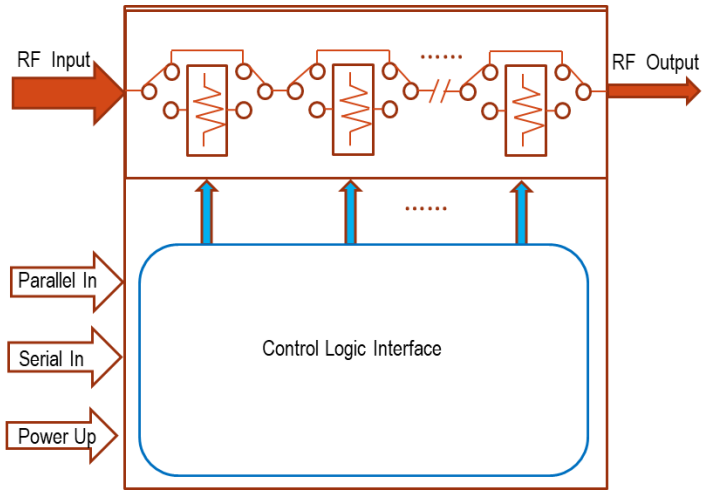


Figure 1

RFone Technology, Inc. www.rfonetech.com All Right Reserved

Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
V_{DD} to GND	-0.3	6.0	V
Vctrl to GND(Parallel Mode)	-0.3	6.0	V
Input Power		30	dBm
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM		1000	V
ESD Voltage– CDM		500	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 2

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	/	2.7	3.3	5.5	V
Operating Temp Range	/	-55	25	125	°C
RF Frequency Range	/	10		4000	MHz
Logic High	/	1.1	3.3	Vdd	V
Logic Low	/	-0.3	0	0.7	V

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Specification

Typical Application Circuit, Normal mode (V_{dd}=3.3V,Vss=0V), T_C = +25°C, Input power = 0dBm.

Table 3

Parameter	Conditions	Min	Typ	Max	Units
Operation Frequency	/	10		4000	MHz
	0.5 dB Step		31.5		
Insertion Loss	10.0MHz - 1.0GHz		1.0		dB
	1.0GHz - 2.2GHz		1.4		
	2.2GHz - 4.0GHz		1.7		
Attenuation Error	10.0MHz - 1.0GHz	±(0.25+6% of attenuation setting)			dB
	1.0GHz - 2.2GHz	±(0.25+5% of attenuation setting)			
	2.2GHz - 4.0GHz	±(0.25+4% of attenuation setting)			
Return Loss	10MHz – 4000MHz	9	14		dB
Input IP3	Pin = 18dBm/tone,20MHz spacing		50		dBm
Input 0.1dB Compression			30		dBm
Switching Time	50% CTRL to 90% RF		80	110	ns
	50% CTRL to 10% RF		80	100	
Logic Input High Threshold		1.1		VDD	V
Logic Input Low Threshold		-0.3		0.6	V
Logic Current	For each control pin		25		μA
DC Current (V_{DD})	3.3V Logic		300		μA
Setting Time	RF settled to within 0.05dB of final value			200	ns

Pin Diagram

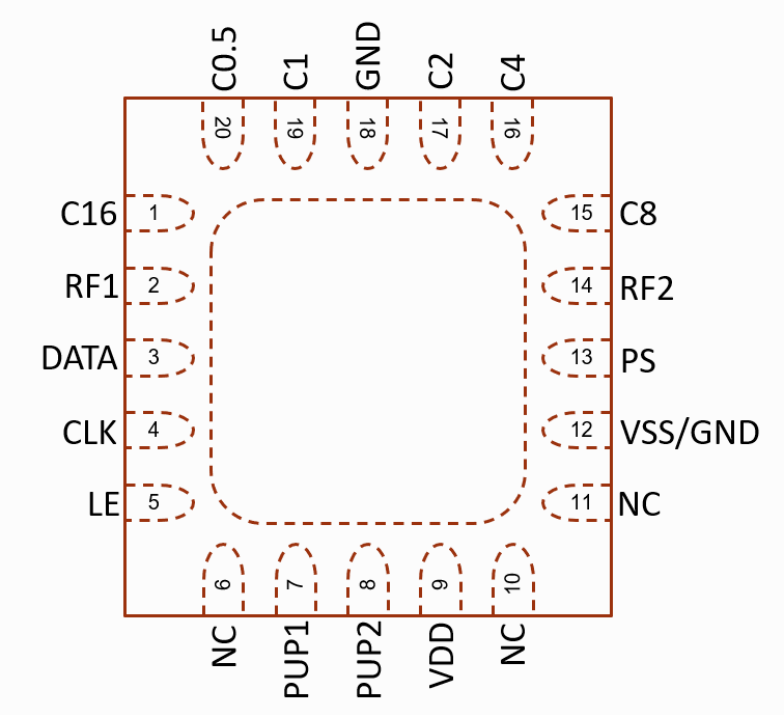


Figure 2

Pin Description

Table 4

Pin No.	Label	Description
1	C16	Parallel Control Bit,16 dB
2	RF1	RF Port
3	DATA	Serial Interface Data Input
4	CLK	Serial Interface Clock Input
5	LE	Serial Interface Latch Enable Input
6	NC	NC
7	PUP1	Power-up selection bit 1
8	PUP2	Power-up selection bit 2
9	VDD	Supply Voltage
10	NC	Ground
11	NC	Ground
12	VSS/GND	External Vss negative voltage control or ground
13	PS	Serial / Parallel Mode Select
14	RF2	RF Port
15	C8	Parallel Control Bit, 8 dB
16	C4	Parallel Control Bit, 4 dB
17	C2	Parallel Control Bit, 2 dB
18	GND	Ground
19	C1	Parallel Control Bit, 1 dB
20	C0.5	Parallel Control Bit, 0.5 dB

Control Logic

Parallel / Serial Selection

Either a Parallel or Serial interface can be used to control the RS15512.The P/S pin provides this selection, with P/S = LOW selecting the Parallel interface and P/S = HIGH selecting the Serial interface.

Parallel Mode Interface

For Latched Parallel Interface Mode, the LE should be LOW while changing attenuation state control values then pulse LE HIGH to LOW to latch new attenuation state into the device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches or jumpers).

Notice: CLK and SI should be connected Ground while the RS15512 is in Parallel Mode Interface.

Table 5 Parallel Mode Attenuation Word Truth Table

Parallel Control Bit Setting							Attenuation Value
PS	C16	C8	C4	C2	C1	C0.5	
0	0	0	0	0	0	0	Reference IL
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

When the attenuator powers us in Parallel mode (P/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in table 6 (Parallel PUP Truth Table)

Table 6 Parallel PUP Truth Table

P/S	LE	PUP1	PUP2	Attenuation State
0	0	0	0	Reference Loss
0	0	1	0	8dB
0	0	0	1	16dB
0	0	1	1	31.5dB
0	1	X	X	Define by C0.5-C16

 All Rights Reserved

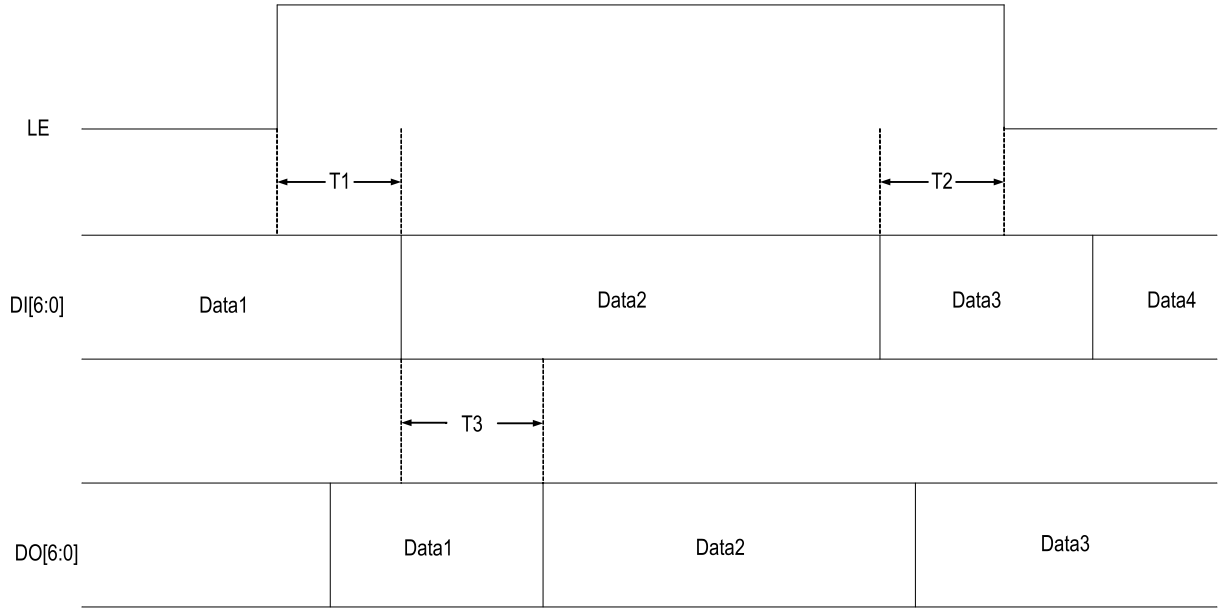


Figure 3 Parallel Mode Timing Diagram

Table 7 Parallel Mode AC Characteristics

Parameter	Min.	Max	Unit
Parallel data setup time, T1	10		ns
Parallel data hold time, T2	10		ns
Parallel data update delay time, T3		10	ns

Serial Mode Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The Serial interface is controlled using three CMOS-compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

It is required that all Parallel control inputs be grounded when the DSA is used in Serial mode.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA.

Table 8 6-Bit Attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) LSB (last in)

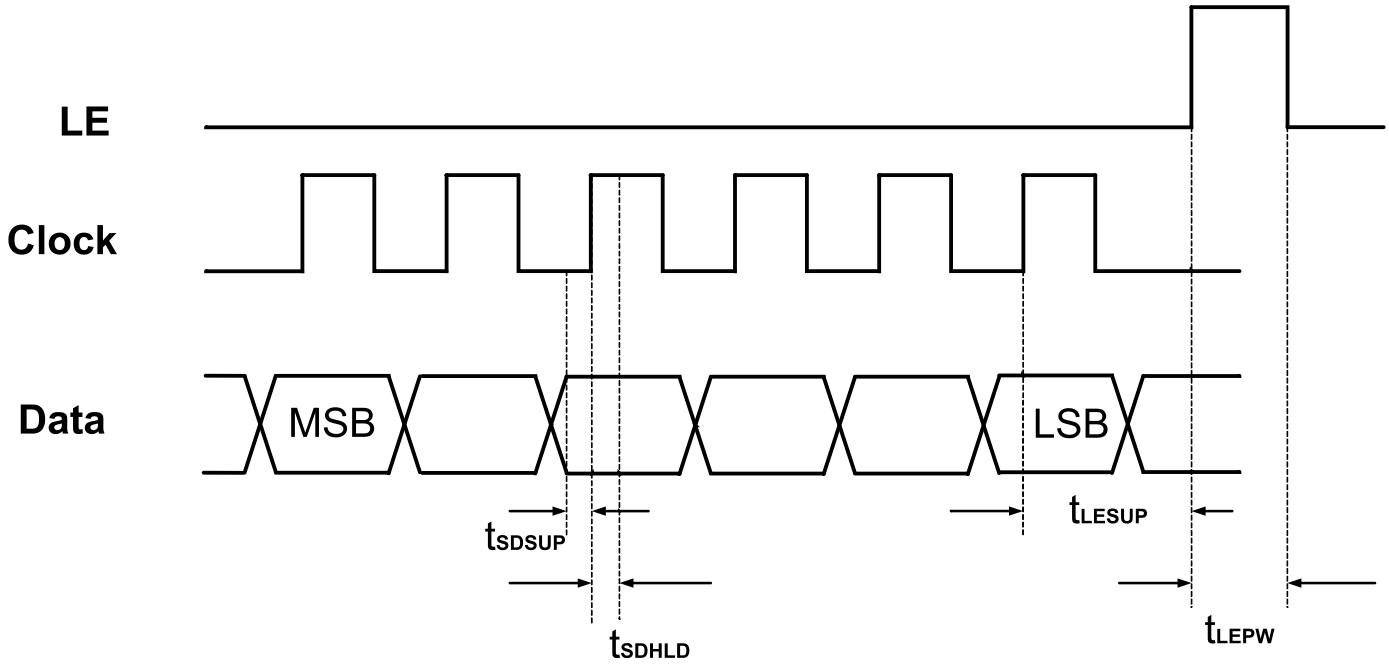


Figure 4 Serial Mode Timing Diagram

Table 9 Serial Mode AC Characteristics

Symbol	Parameter	Min.	Max	Unit
f_{Clk}	Serial data clock frequency		10	MHz
t_{ClkH}	Serial clock HIGH time	30		ns
t_{ClkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock rising edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock rising edge	10		ns

Typical Performance Data, Vdd=3.3V, Vss=0V

Figure 5 Insertion Loss VS Frequency @ Major Attenuation Steps

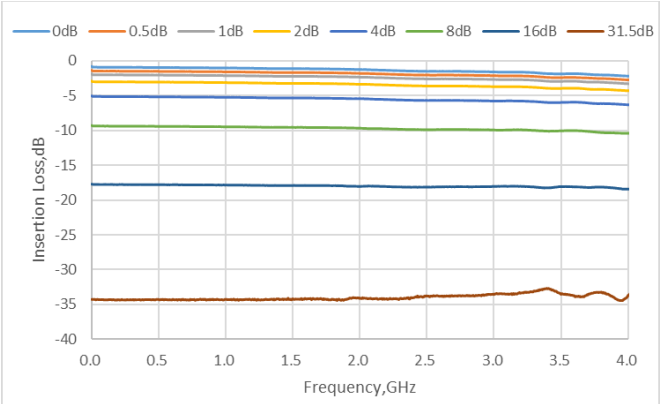


Figure 6 Insertion Loss VS Temperature

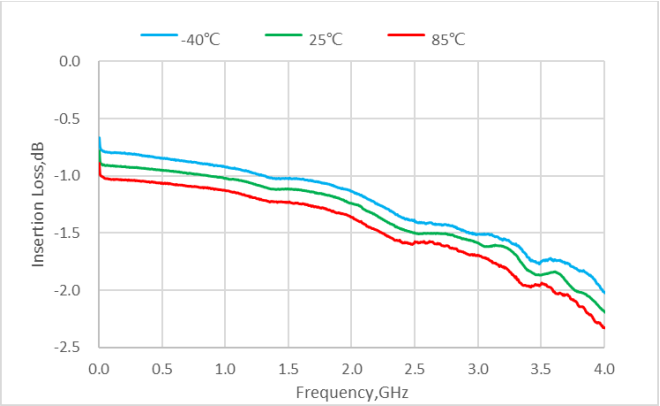


Figure 7 Input Return Loss VS Frequency @ Major Attenuation Steps

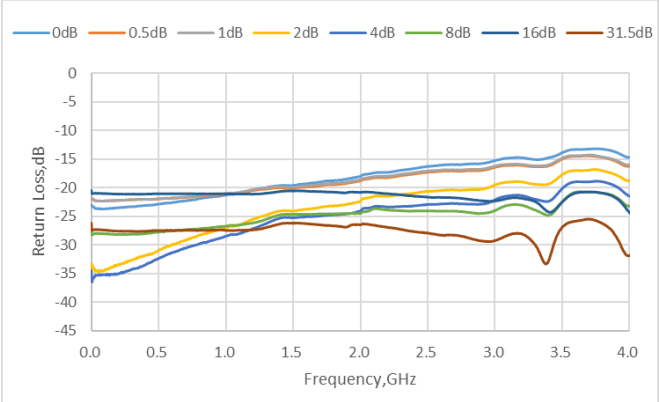


Figure 8 Input Return Loss VS Temperature

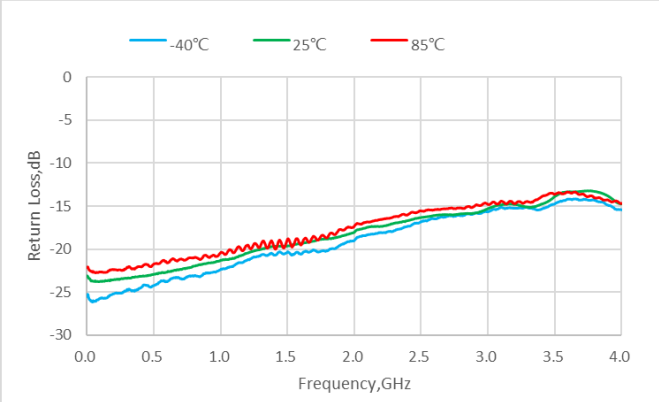


Figure 9 Output Return Loss VS Frequency @ Major Attenuation Steps

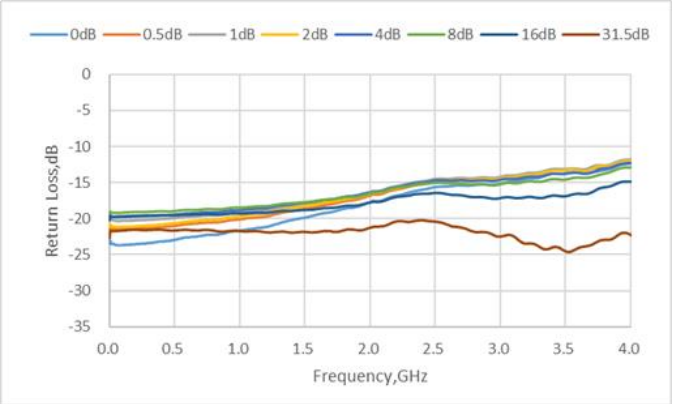
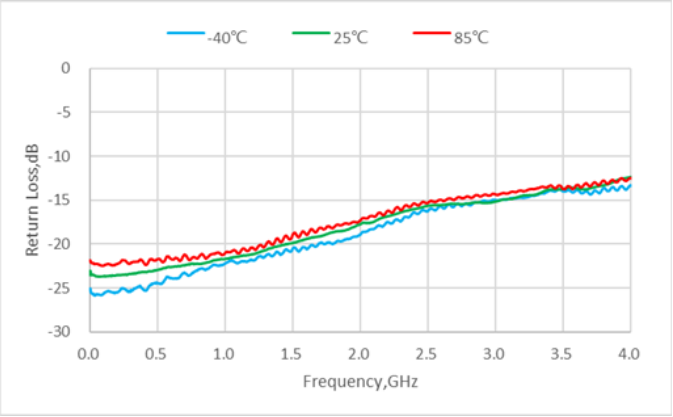


Figure 10 Output Return Loss VS Temperature



Typical Performance Data, Vdd=3.3V, Vss=0V

Figure 11 Attenuation Error VS Frequency @ Major Attenuation Steps

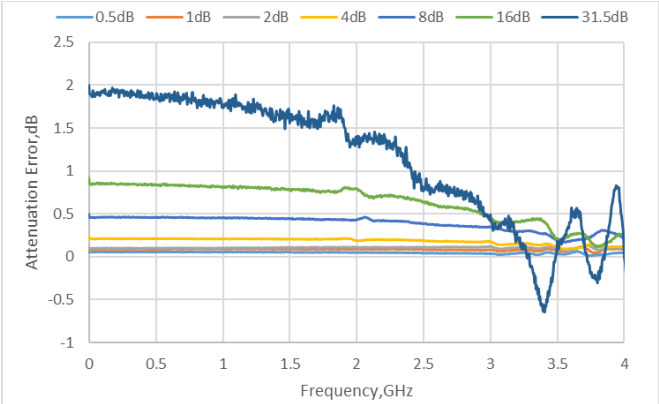


Figure 12 Attenuation Error VS Attenuation Setting

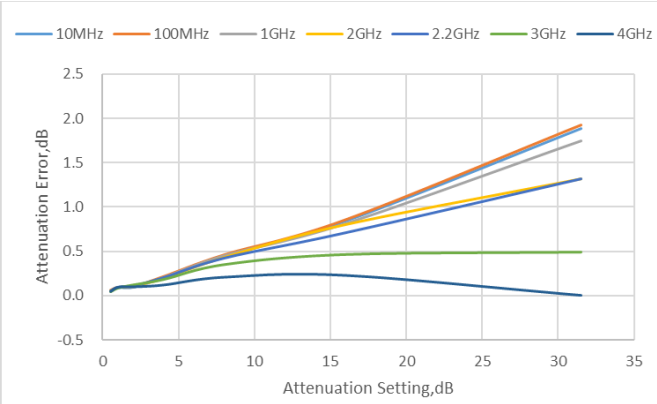


Figure 13 Actual Attenuation VS Ideal Attenuation

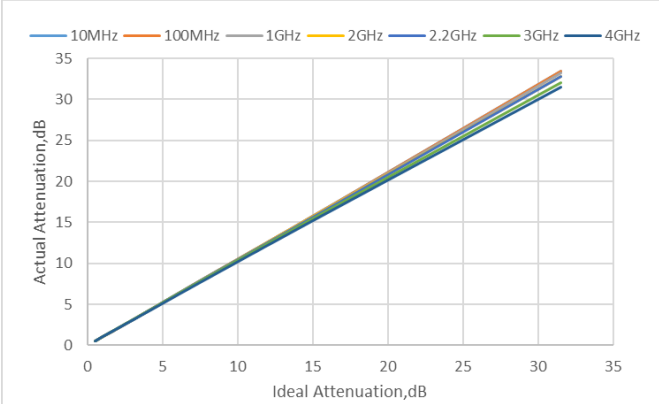


Figure 14 Relative Phase Error VS Frequency @ Major Attenuation Steps

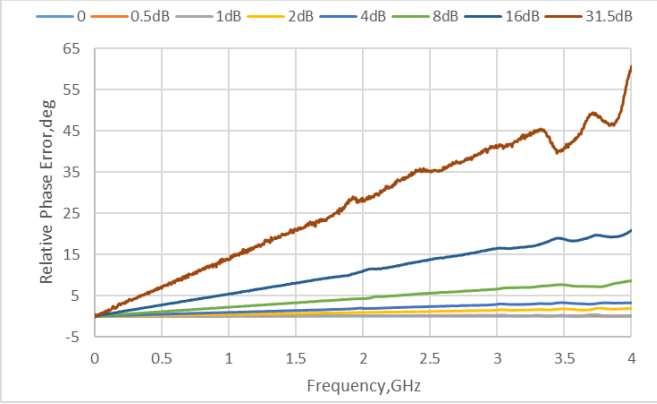


Figure 15 Attenuation Error @ 10MHz VS Temperature

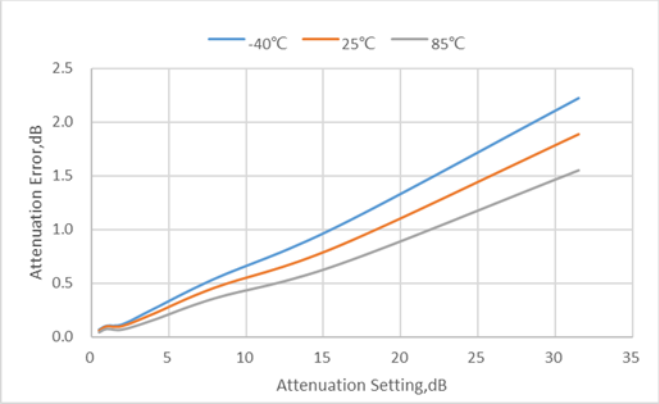
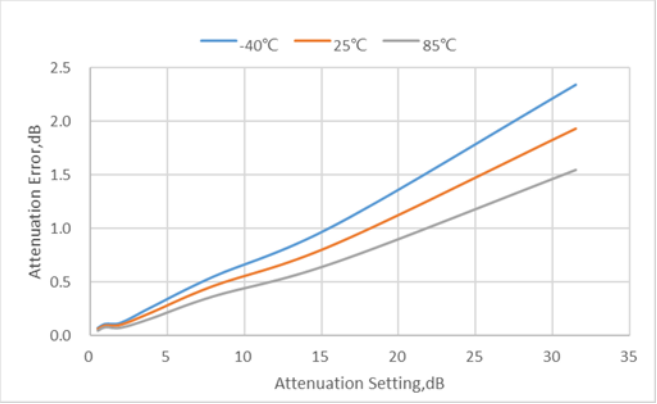


Figure 16 Attenuation Error @ 100MHz VS Temperature



Typical Performance Data, Vdd=3.3V, Vss=0V

Figure 17 Attenuation Error @ 1GHz VS Temperature

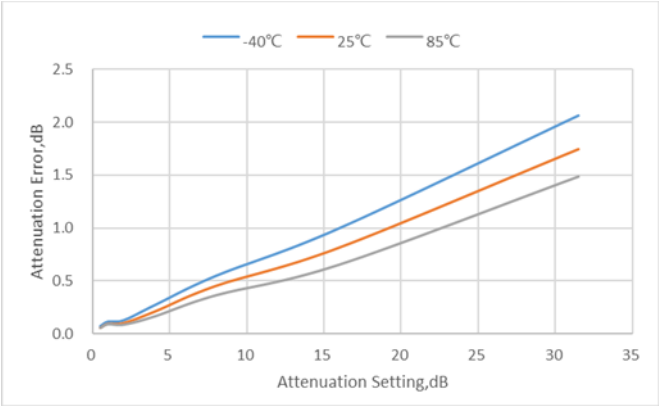


Figure 18 Attenuation Error @ 2.2GHz VS Temperature

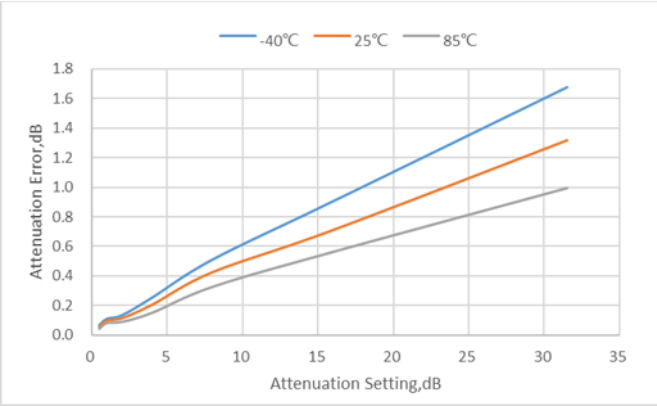


Figure 19 Attenuation Error @ 3GHz VS Temperature

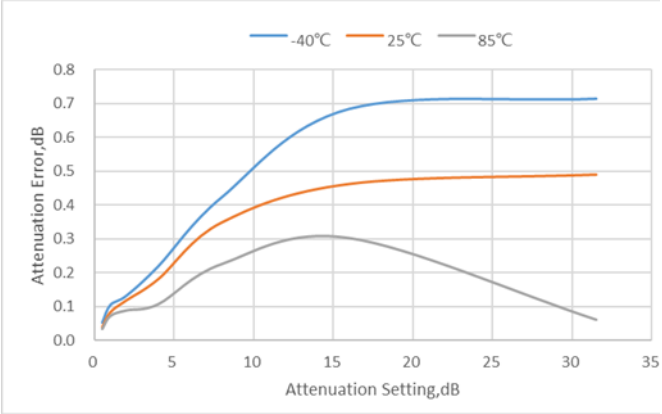


Figure 20 Attenuation Error @ 4GHz VS Temperature

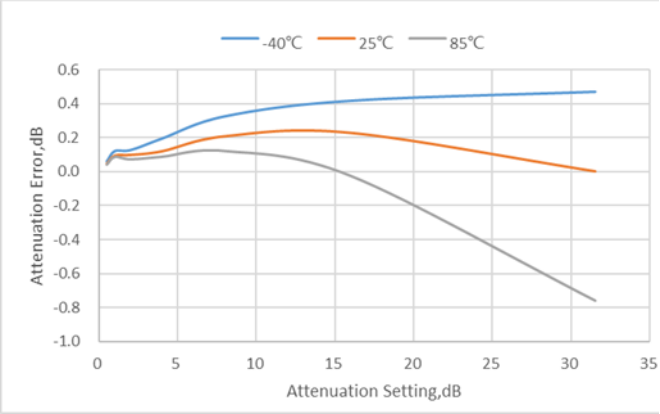


Figure 21 Spur Vdd=3.3V, Vss=0V

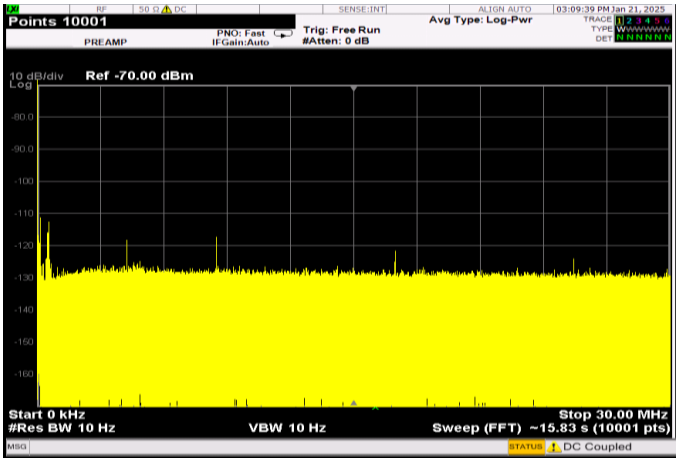
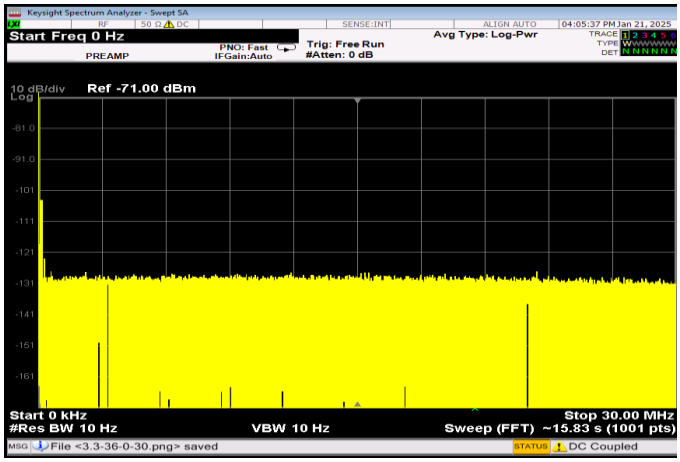


Figure 22 Spur Vdd=3.3V, Vss=-3.3V



Application Information

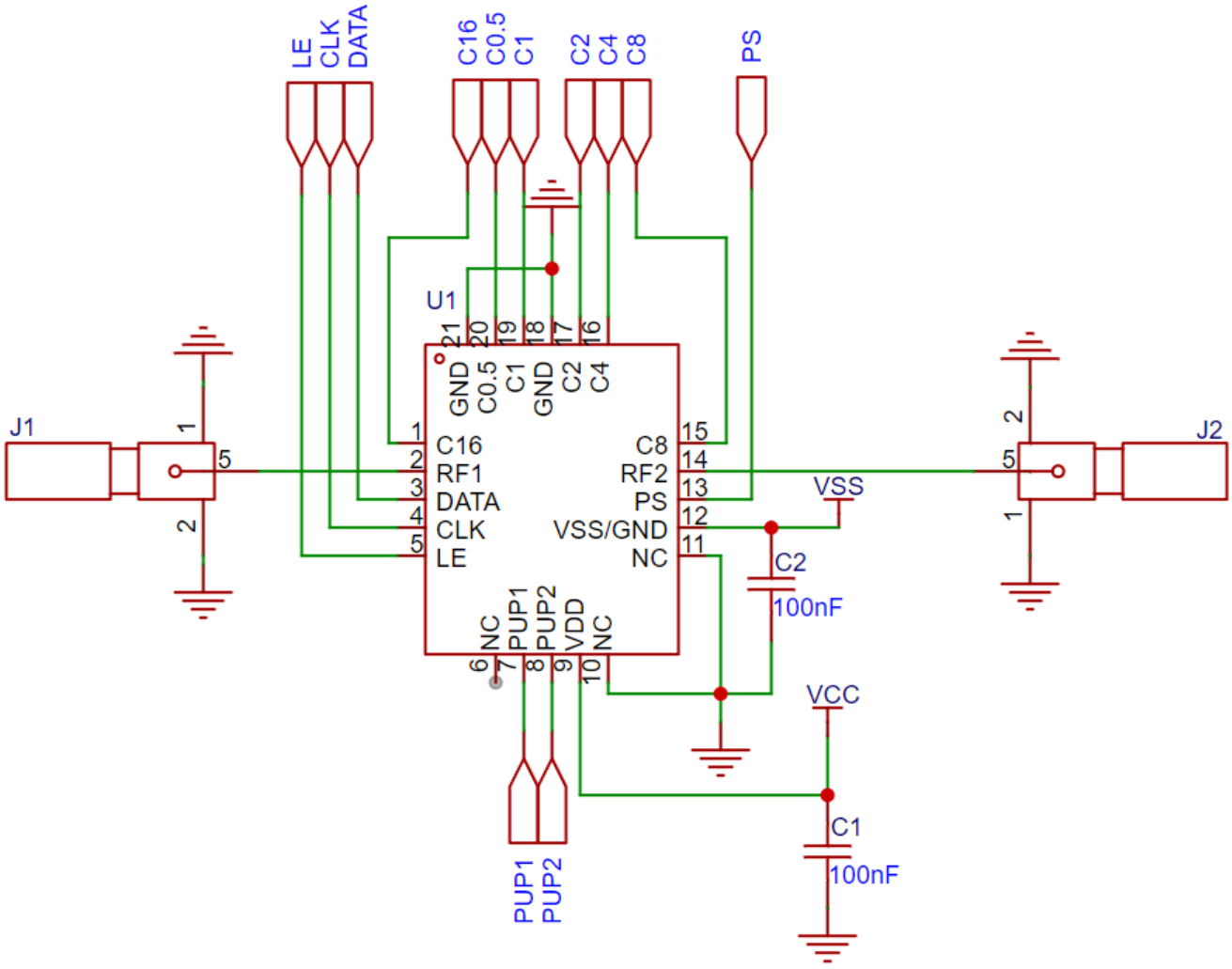


Figure 23

Package Drawing

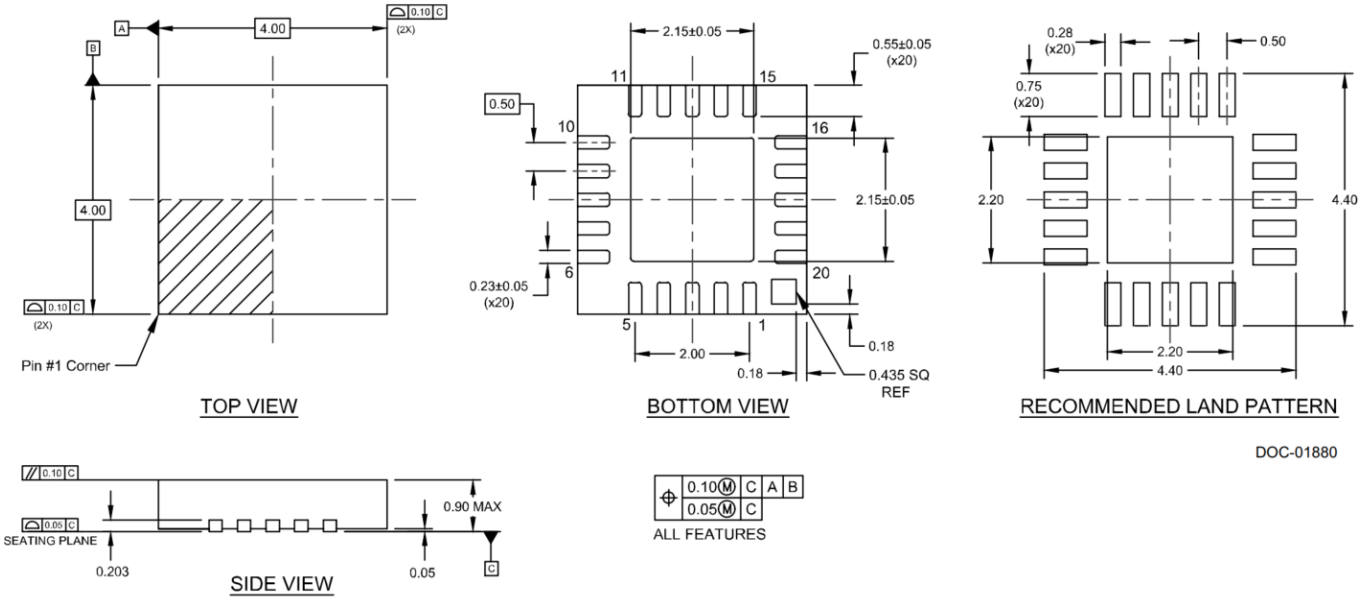


Figure 24

Revision History

Table 10

Revision Number	Revision Date	Description	Modifications
0	2022/11/7	Draft	—
0.1	2023/7/11	Preliminary Specification	
0.2	2024/3/10		Update
0.3	2025/6/11		Update

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. RFone Technology reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event RFone Technology decides to change the specifications, RFone Technology will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@rfonetech.com.

Disclaimers

The information in this document is believed to be reliable. However, RFone Technology assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. RFone Technology 's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the RFone Technology product could create a situation in which personal injury or death might occur. RFone Technology assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

RFone Technology products are protected under one or more of the following Chinese patents.For details, visit patents.rfonetech.com

Copyright and Trademark

©2019 – 2025, RFone Technology Inc. All rights reserved. The RFone Technology name, logo are registered trademarks.