Specification

RS15511A Digital Step Attenuator

General Description

The RS15511A is a 7-bit digital step attenuator (DSA). It is available in a 4 mm × 4 mm, 24-lead QFN and provides 31.75dB attenuation range in 0.25dB,0.5dB and 1dB steps from 9 kHz to 8 GHz.

The RS15511A incorporates a negative voltage generator to operate with a single positive supply voltage from 2.7 V to 5.5 V applied to the VDD pin when all the GND pins are all connected to ground. The RS15511A provides both serial and parallel digital control interface.

Applications

- 3G/4G/5G wireless infrastructure
- Test equipment
- Land mobile radio system
- Point to point communication system

Features

- **Excellent RF Performance**
  - Flexible attenuation steps of 0.25dB, 0.5dB and 1dB up to 31.75dB
  - High Attenuation Accuracy and Low Insertion Loss
- **High input linearity**
  - P0.1dB: 30 dBm typical
  - Third-order intercept (IP3): 50 dBm typical
- **Programming interface**
  - Parallel
  - Serial

Functional Block Diagram

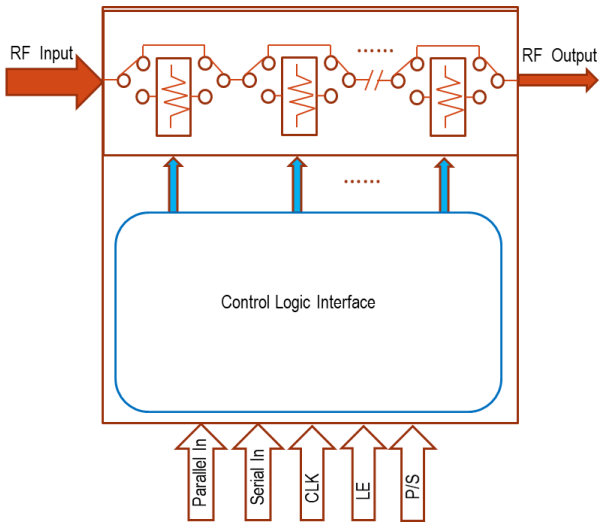


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
V_{DD} to GND	-0.3	5.5	V
Vctrl to GND (Parallel Mode)	-0.3	5.5	V
Input Power		30	dBm
Storage Temperature Range	-60	150	°C
ESD Voltage– HBM		1000	V
ESD Voltage– CDM		500	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 2

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	/	2.8	3.3	5.5	V
Operating Temp Range	/	-40	25	105	°C
RF Frequency Range	/	0.009		8000	MHz
Logic High	/	1.2	3.3	Vdd	V
Logic Low	/	-0.3	0	0.7	V

Operation should be restricted to the limits in the Recommended Operating Conditions table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Specification

Typical Application Circuit, Normal mode (V_{DD}=3.3V), T_C = +25°C, Input power = 0dBm.

Table 3

Parameter	Conditions	Min	Typ	Max	Units
Operation Frequency	/	0.009		8000	MHz
Attenuation Range	0.25 dB Step		31.75		dB
	0.5 dB Step		31.50		
	1 dB Step		31.00		
Insertion Loss	9.0KHz - 1.0GHz		0.8		dB
	1.0GHz - 3.0GHz		1.3		
	3.0GHz - 4.0GHz		1.6		
	4.0GHz - 6.0GHz		2.4		
	6.0GHz - 8.0GHz		3.2		
Attenuation Accuracy	0.25dB Step				dB
	9.0KHz - 1.0GHz	±(0.1+2.3% of attenuation setting)			
	1.0GHz - 3.0GHz	±(0.15+2.6% of attenuation setting)			
	3.0GHz - 4.0GHz	±(0.2+3.6% of attenuation setting)			
	4.0GHz - 6.0GHz	±(0.2+4.6% of attenuation setting)			
	0.5dB Step				
	9.0KHz - 1.0GHz	±(0.25+2.5% of attenuation setting)			
	1.0GHz - 3.0GHz	±(0.25+2.7% of attenuation setting)			
	3.0GHz - 4.0GHz	±(0.35+3.5% of attenuation setting)			
	4.0GHz - 5.0GHz	±(0.35+4.0% of attenuation setting)			
	5.0GHz - 7.0GHz	±(0.4+4.5% of attenuation setting)			
	1dB Step				
	9.0KHz - 1.0GHz	±(0.35+2.6% of attenuation setting)			
	1.0GHz - 3.0GHz	±(0.3+2.7% of attenuation setting)			
	3.0GHz - 4.0GHz	±(0.25+4.5% of attenuation setting)			
	4.0GHz - 6.0GHz	±(0.4+5% of attenuation setting)			
	6.0GHz - 8.0GHz	±(0.5+5% of attenuation setting)			
Return Loss	9kHz – 8000MHz	12	15		dB
Input IP3	Pin = 18dBm/tone,20MHz spacing,2.5 - 4.0GHz		50		dBm
Input 0.1dB Compression		23	29		dBm
Glitch	After switching attenuation state 100ns		0.1	0.4	dB
Delay			5	10	ns
Switching Time	50% CTRL to 90% RF		80	110	ns
	50% CTRL to 10% RF		80	100	
Logic Input High Threshold		1.1		VDD	V
Logic Input Low Threshold		-0.3		0.6	V
Logic Current	For each control pin		25		μA
DC Current (V_{DD})	3.3V Logic		310		μA
Setting Time	RF settled to within 0.05dB of final value		1	1.6	us

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Pin Diagram

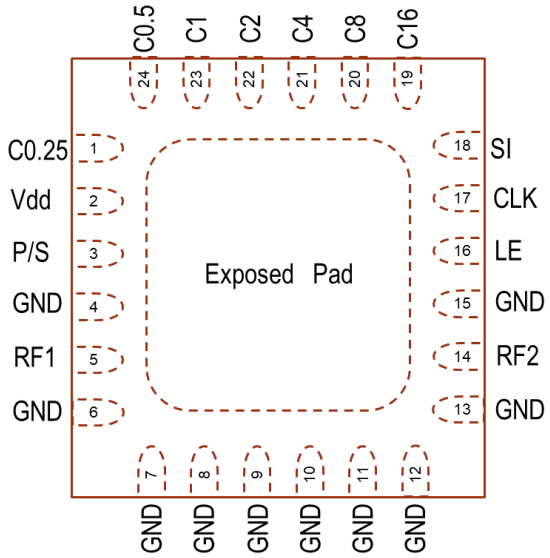


Figure 2

Pin Description

Table 4

Pin No.	Label	Description
1	C0.25	Parallel Control Bit, 0.25 dB
2	Vdd	Supply Voltage
3	P/S	Serial / Parallel Mode Select
4,6 - 13,15,	GND	Ground
5	RF1	RF Port (RF Input)
14	RF2	RF Port (RF Output)
16	LE	Serial Interface Latch Enable Input
17	CLK	Serial Interface Clock Input
18	SI	Serial Interface Data Input
19	C16	Parallel Control Bit, 16 dB
20	C8	Parallel Control Bit, 8 dB
21	C4	Parallel Control Bit, 4 dB
22	C2	Parallel Control Bit, 2 dB
23	C1	Parallel Control Bit, 1 dB
24	C0.5	Parallel Control Bit, 0.5 dB
	Pad	GND

Control Logic

Parallel / Serial Selection

Either a Parallel or Serial interface can be used to control the RS15511A.The P/S pin provides this selection, with P/S = LOW selecting the Parallel interface and P/S = HIGH selecting the Serial interface.

Parallel Mode Interface

For Latched Parallel Interface Mode, the LE (PIN16) should be LOW while changing attenuation state control values then pulse LE HIGH to LOW to latch new attenuation state into the device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches or jumpers).

Notice: CLK and SI should be connected Ground while the RS15511A is in Parallel Mode Interface.

Table 5 Parallel Mode Attenuation Word Truth Table

Parallel Control Bit Setting							Attenuation Value
C16	C8	C4	C2	C1	C0.5	0.25	
L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

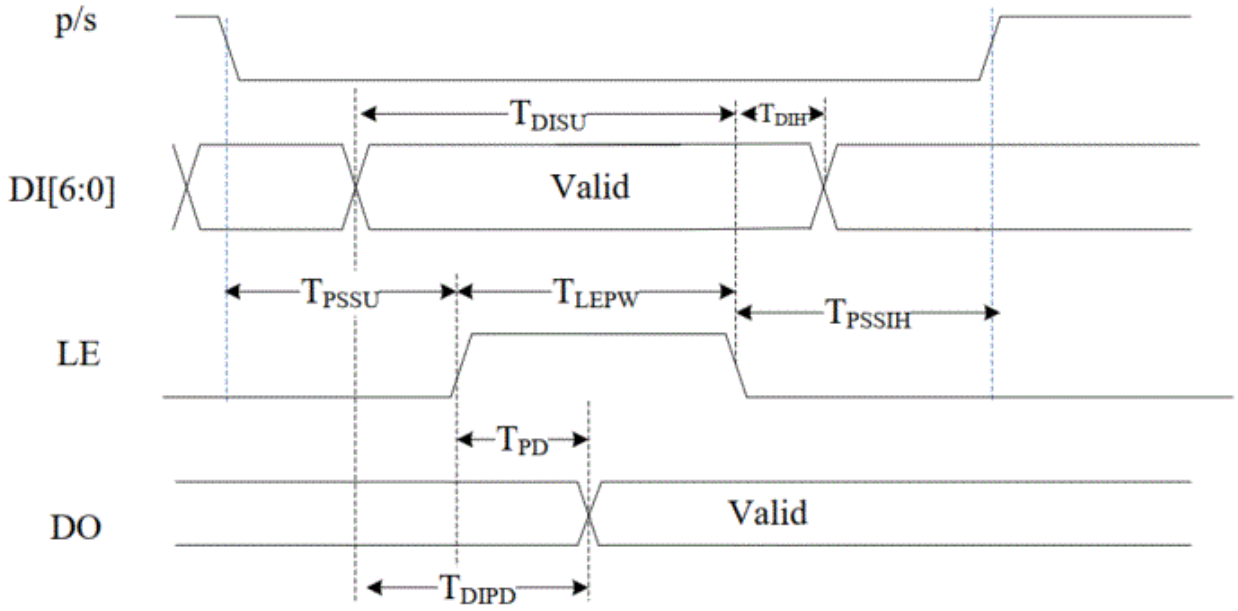


Figure 3 Parallel Mode Timing Diagram

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Table 6 Parallel Mode AC Characteristics

Parameter	Min.	Max	Unit
Latch Enable minimum pulse width, T_{LEPW}	30		ns
Parallel data hold time, T_{DIH}	100		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel / Serial setup time, T_{PSSU}	100		ns
Parallel / Serial hold time, T_{PSIH}	100		ns
Digital register delay time, T_{PD}		10	ns
Digital register delay time (direct mode), T_{DIPD}		5	ns

Serial Mode Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The Serial interface is controlled using three CMOS-compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

It is required that all Parallel control inputs be grounded when the DSA is used in Serial mode.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA.

Table 7 Serial Mode Attenuation Word Truth Table

Serial Control Bit Setting								Attenuation Value
D7	D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	L	Reference IL
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

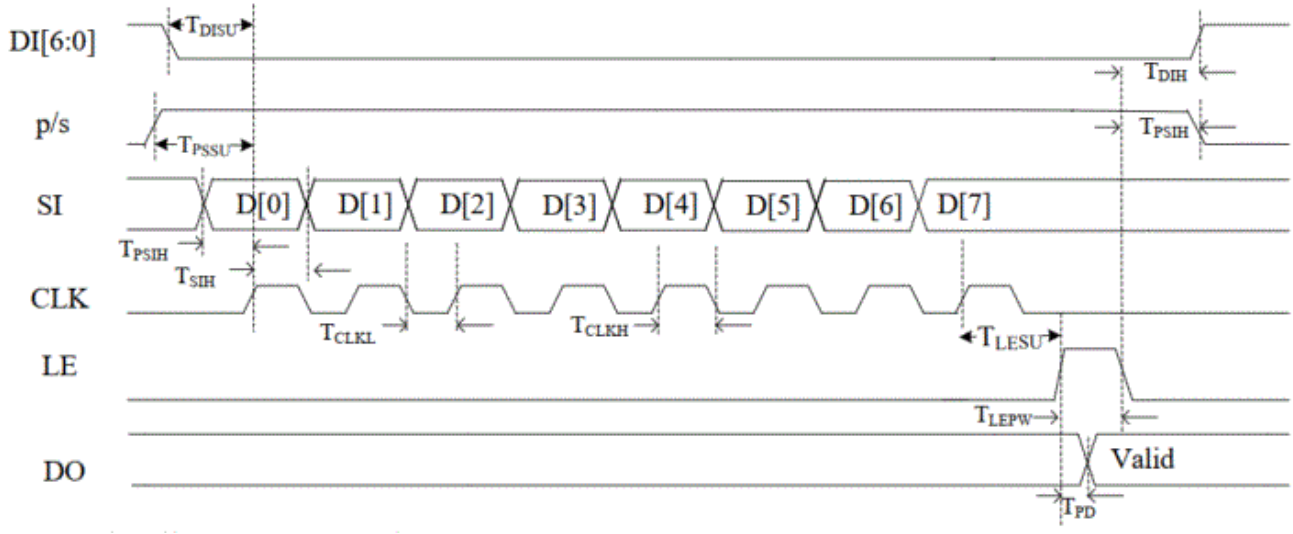


Figure 4 Serial Mode Timing Diagram

Table 8 Serial Mode AC Characteristics

Parameter	Min.	Max	Unit
Latch Enable minimum pulse width, T_{LEPW}	30		ns
Serial clock frequency, F_{CLK}		10	MHz
Serial clock HIGH time, T_{CLKH}	30		ns
Serial clock LOW time, T_{CLKL}	30		ns
Last Serial clock rising edge setup time to LE rising edge, T_{LESU}	10		ns
Serial data hold time, T_{SIH}	10		ns
Serial data setup time, T_{SISU}	10		ns
Parallel data hold time, T_{DIH}	100		ns
Parallel data setup time, T_{DISU}	100		ns
Parallel / Serial setup time, T_{PSSU}	100		ns
Parallel / Serial hold time, T_{PSIH}	100		ns
Digital register delay time, T_{PD}		10	ns

Typical Performance Characteristics

Figure 5. Insertion Loss

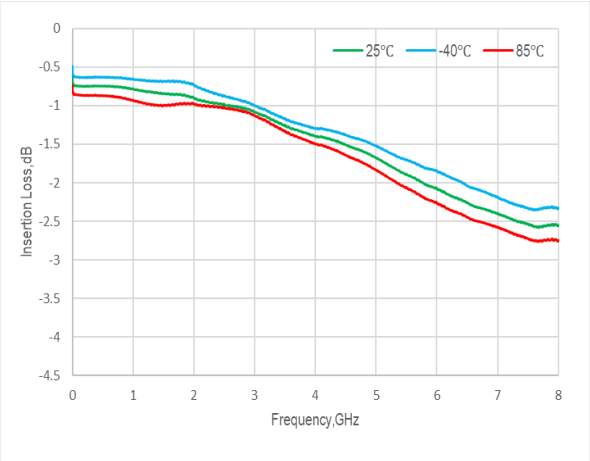


Figure 6. Relative Phase VS Attenuation Value

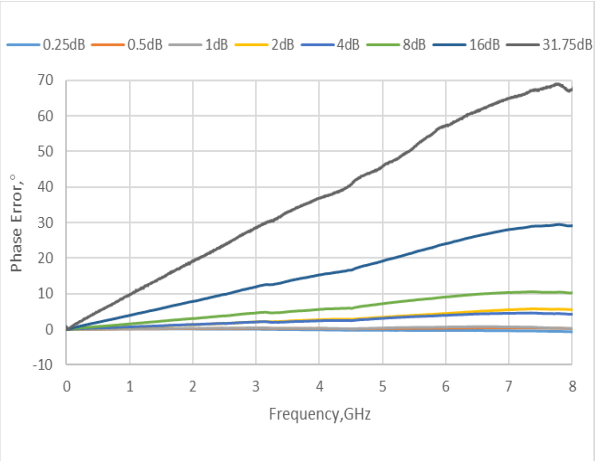


Figure 7. Return Loss RF1

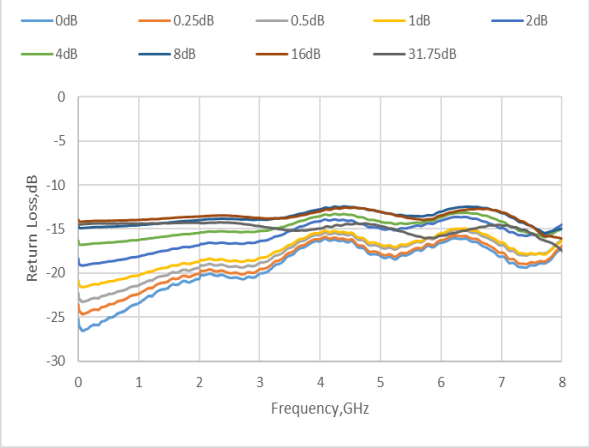


Figure 8. Return Loss RF2

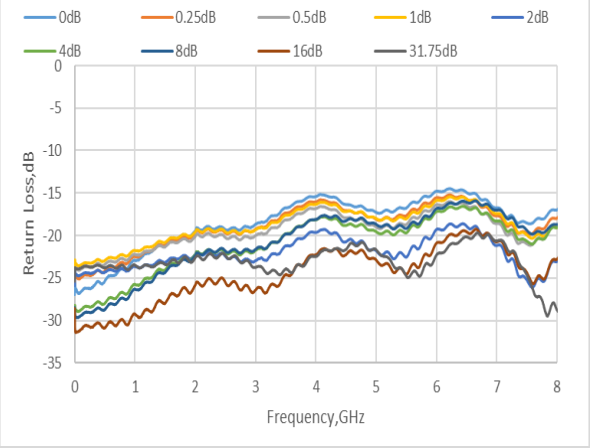


Figure 9. Attenuation Error VS Frequency

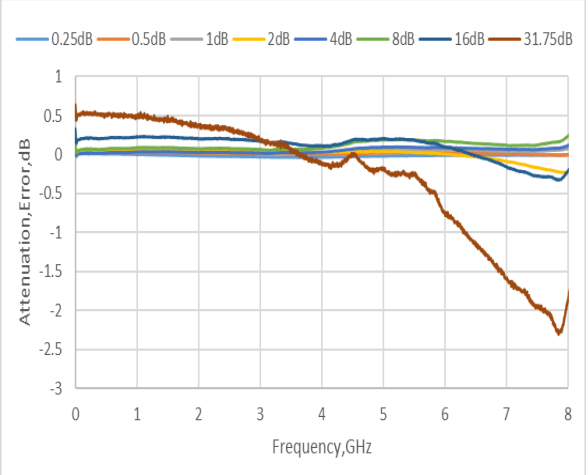
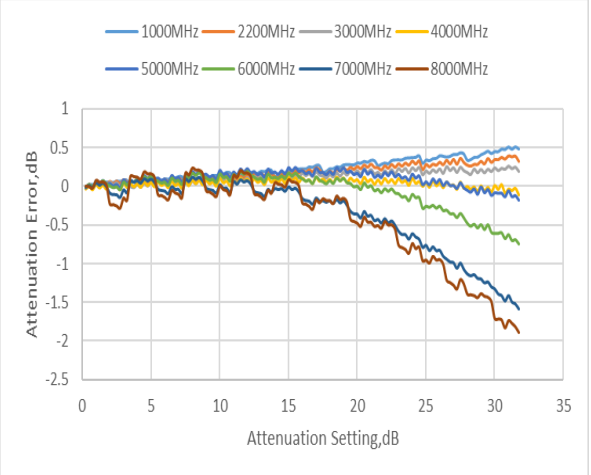


Figure 10. Attenuation Error VS Attenuation Setting



Application Information

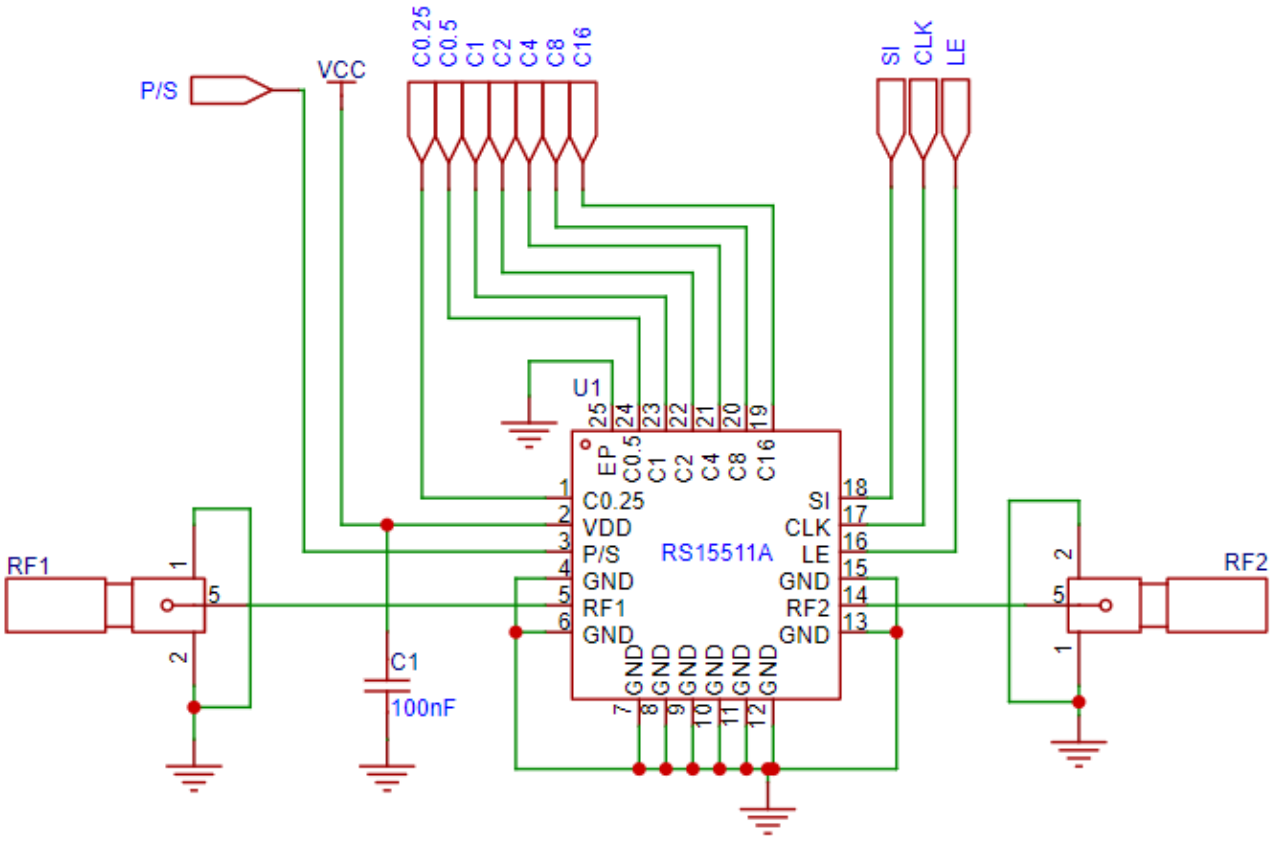


Figure 11

Package Drawing

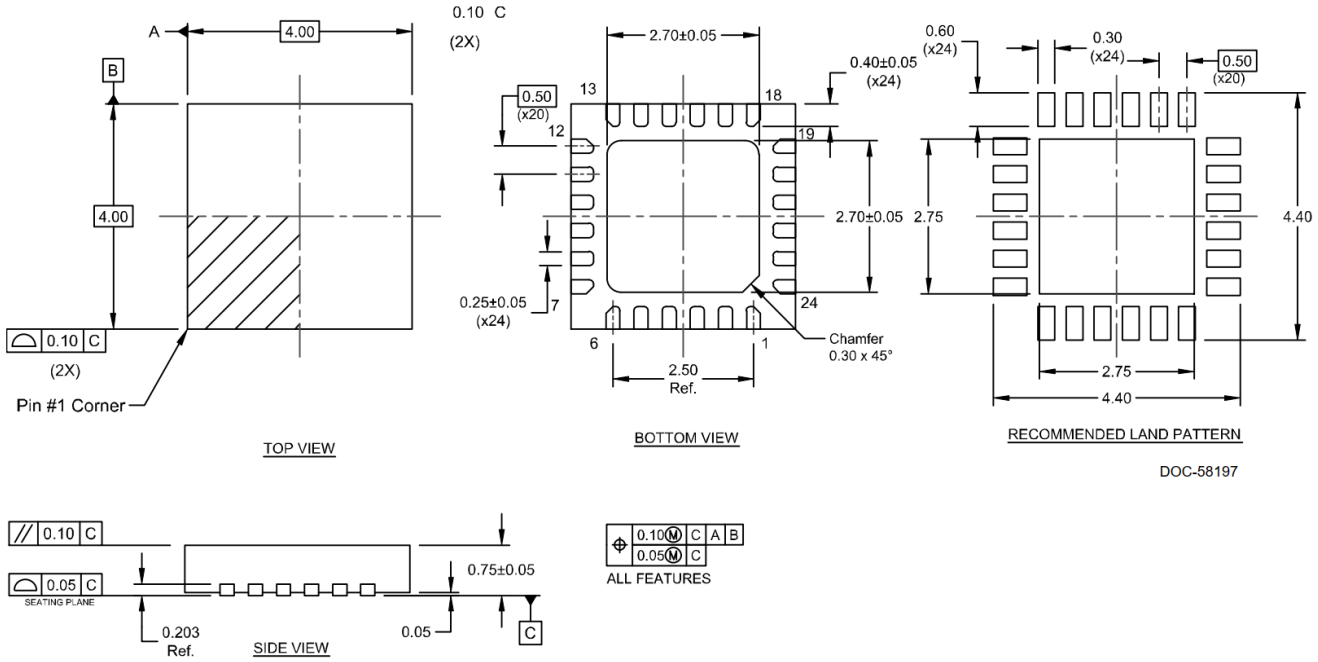


Figure 12

Revision History

Table 9

Revision Number	Revision Date	Description	Modifications
0	2022/11/7	Draft	—
0.1	2023/3/9	Initial release	Update RF Specification
0.2	2023/7/18	Preliminary	
0.3	2023/12/5		Frequency Range:8GHz
0.4	2025/5/15		
0.5	2025/9/15		

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. RFone Technology reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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