Product Specification

RS1423 Small Size SPDT

General Description

The RS1423 is a silicon-based, high power, low insertion loss, 700 MHz to 6.0 GHz, single-pole, double-throw (SPDT) reflective switch in a 6 leads 1.1x0.7mm Package. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using single-pin control inputs. Using a nominal +3-volt power supply voltage, a typical input 0.1dB compression point of +31 dBm can be achieved.

Features

- Reflective, 50 Ω design
- High input 0.1 dB compression point of 31dBm
- Low insertion loss:
  - 0.38 dB typical to 1.0 GHz
  - 0.7 dB typical to 6.0 GHz
- Isolation of 35dB at 1.0GHz
- High ESD tolerance of 2000V HBM
- Single positive supply: 1.8 – 3.3 V
- Ultra-small 6 leads 1.1x0.7mm package

Applications

- IoT
- WiFi
- General application

Functional Block Diagram

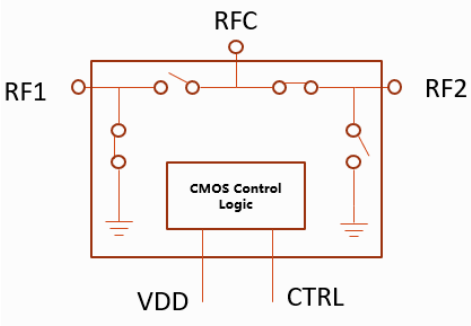


Figure 1

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Absolute Maximum Ratings

Table 1

Parameter	Min	Max	Units
VDD to GND	1.6	4.5	V
CTRL to GND	0	3.3	V
Input Power (50ohm)		31	dBm
Storage Temperature Range	-65	150	°C
ESD Voltage– HBM (Per JESD22-A114)		2000	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Recommended Operating Conditions

Table 2

Parameter	Min	Typical	Max	Unit
Supply Voltage (VDD)	2.4	3	3.5	V
IDD Power Supply Current		45		uA
Operating Temp Range	-40	25	85	°C
Control Logic High Voltage	1.2		VDD	V
Control Logic Low Voltage			0.4	V

Specification

Typical Application Circuit, Normal mode (VDD=3V), T_C = +25°C, F_{RF} = 700MHz, Input power = 20dBm per tone unless otherwise stated. PCB board trace and connector losses are de-embedded unless otherwise noted.

Table 3

Parameter	Conditions	Min	Typ	Max	Units
Insertion Loss	700MHz-1000MHz		0.35		dB
	1000MHz-2000MHz		0.4		
	2000MHz-3000MHz		0.45		
	3000MHz-4000MHz		0.48		
	4000MHz-5000MHz		0.55		
	5000MHz-6000MHz		0.7		
Isolation RFC to RFX	700MHz-1000MHz		40		dB
	1000MHz-2000MHz		30		
	2000MHz-3000MHz		30		
	3000MHz-4000MHz		25		
	4000MHz-5000MHz		20		
	5000MHz-6000MHz		15		
Isolation RFX to RFX	700MHz-1000MHz		42		dB
	1000MHz-2000MHz		32		
	2000MHz-3000MHz		30		
	3000MHz-4000MHz		25		
	4000MHz-5000MHz		20		
	5000MHz-6000MHz		18		
Return Loss (RFC)	700MHz-1000MHz		30		dB
	1000MHz-2000MHz		28		
	2000MHz-3000MHz		28		
	3000MHz-4000MHz		35		
	4000MHz-5000MHz		30		
	5000MHz-6000MHz		25		
Return Loss (RFX)	700MHz-1000MHz		35		dB
	1000MHz-2000MHz		35		
	2000MHz-3000MHz		30		
	3000MHz-4000MHz		28		
	4000MHz-5000MHz		28		
	5000MHz-6000MHz		22		
Input 0.1dB Compression	700MHz		31		dBm
Input IP3	720MHz&780MHz, 20dBm input power		56		dBm
Switching Time	50% CTRL to 90% RF		0.5		us
	50% CTRL to 10% RF		0.6		

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Pin Diagram

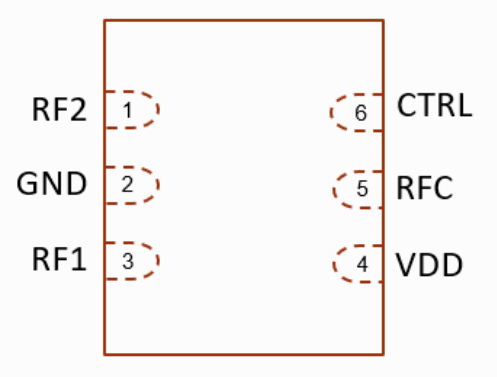


Figure 2

Pin Description

Table 4

Pin No.	Pin Name	Description
1	RF2	RF port 2.
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF1	RF port 1
4	VDD	Power Supply
5	RFC	RF common.
6	CTRL	Control the path of switch

Control Logic

Table 5

Control Voltages	Signal Path
Pin 6 (CTRL) = High	RFC to RF2
Pin 6 (CTRL) = Low	RFC to RF1

Applications Information

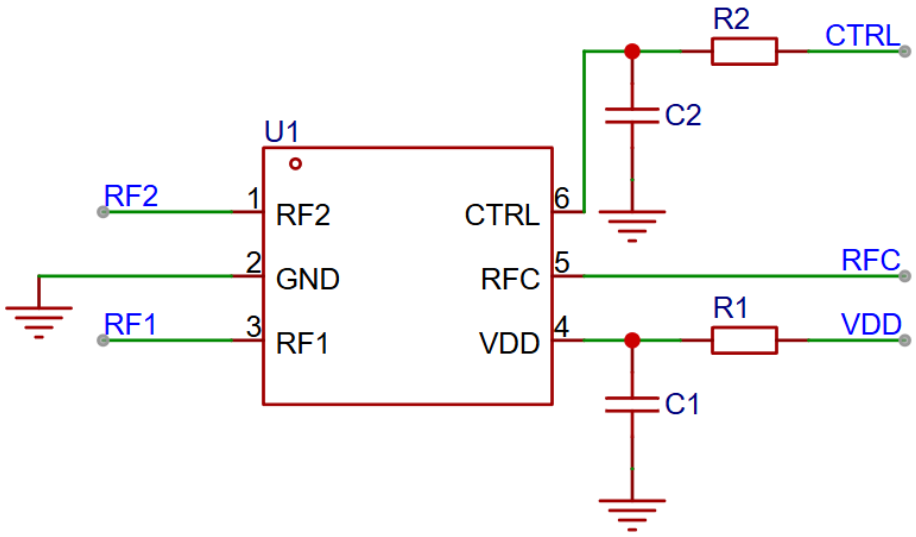


Figure 3

Table 6

No.	Designator	Comment	Footprint
1	C1	100nF	C0402
2	C2	100pF	C0402
3	R1、R2	0 Ω	C0402
4	U1	RS1423	

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Typical Performance Characteristics

Figure 4. Insertion Loss

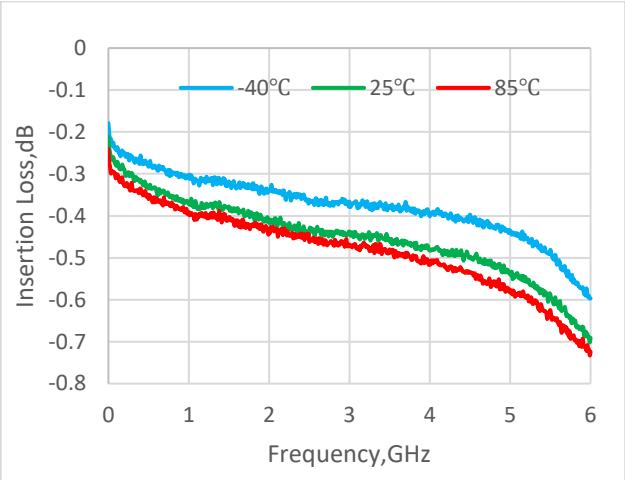


Figure 5. RFC Return Loss

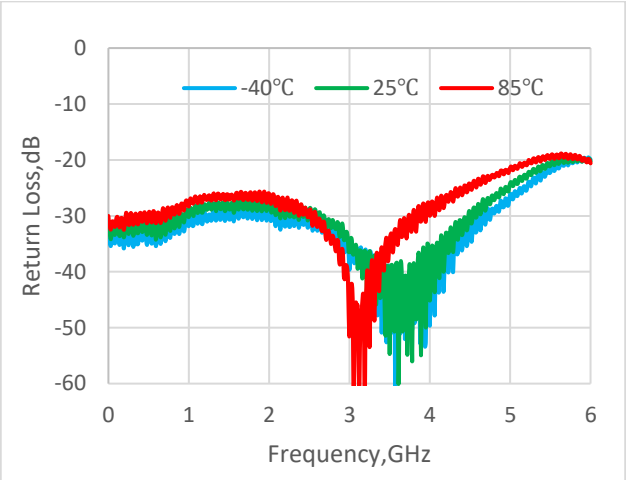


Figure 6. RFX Return Loss

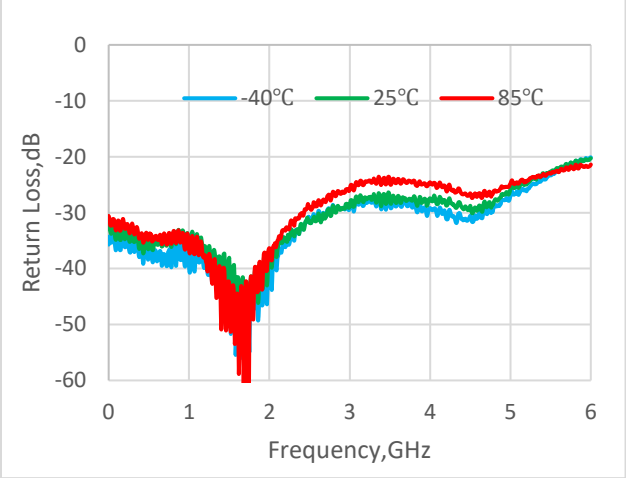


Figure 7. RFC–RFX Isolation

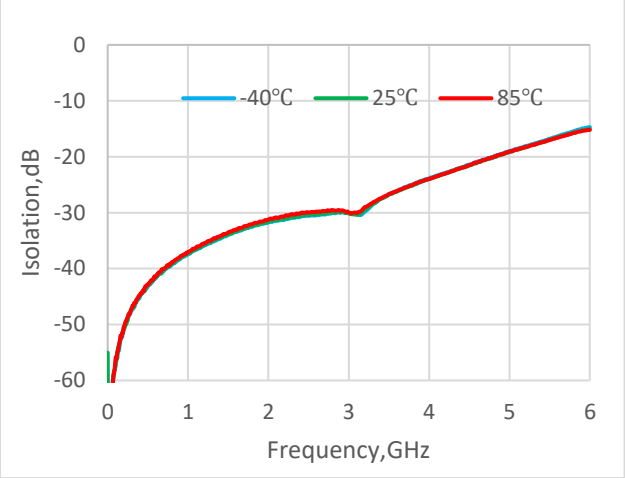


Figure 8. RFX–RFX Isolation

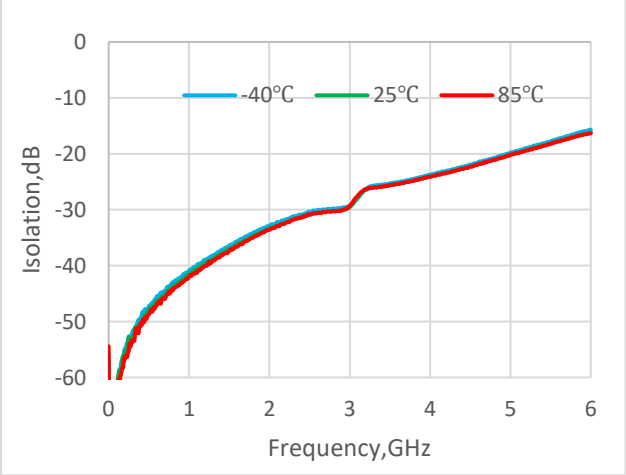
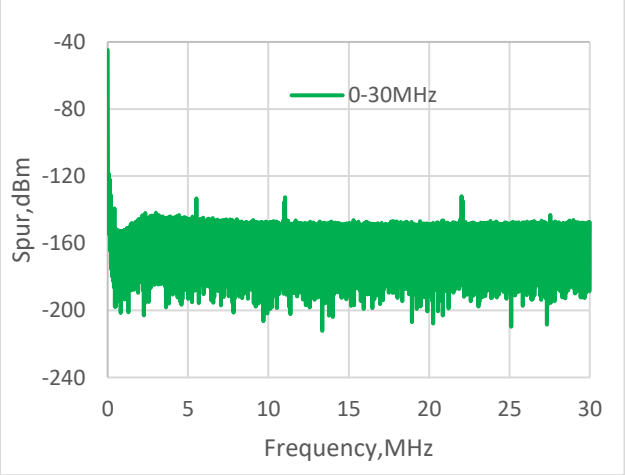


Figure 9. Spur(0-30MHz) ***



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Figure 10. Spur(30-100MHz) ***

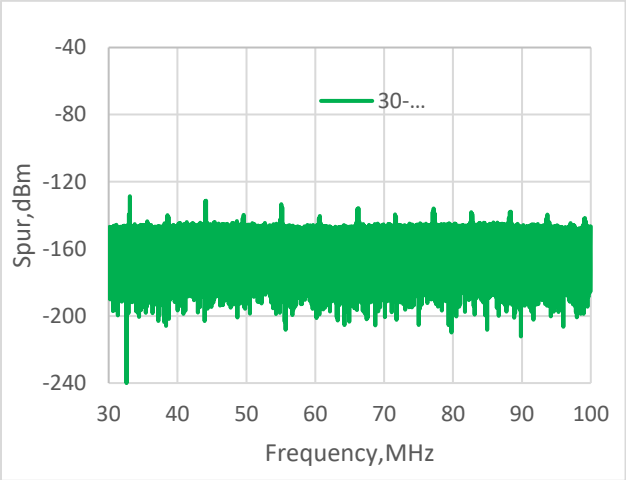
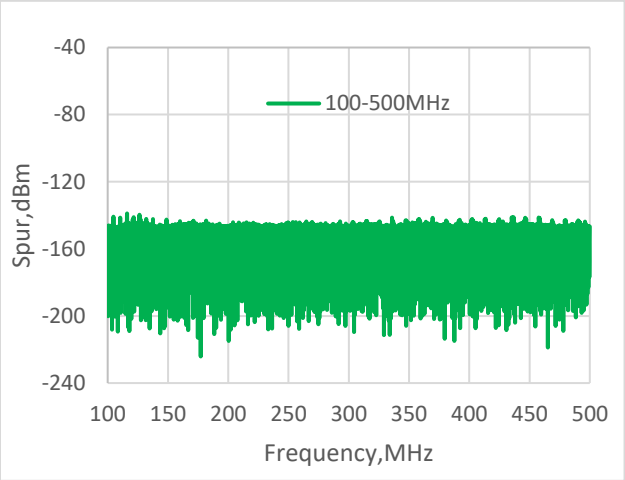
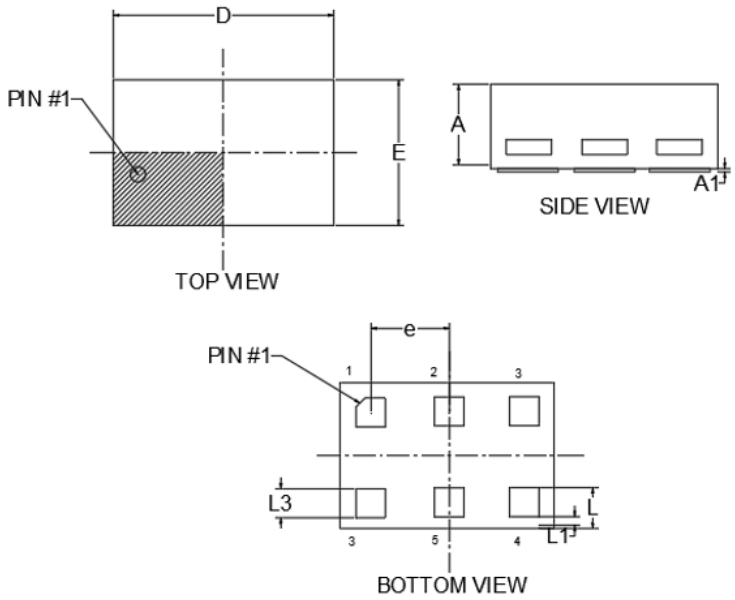


Figure 11. Spur(100-500MHz) ***



*Note:*** spur's test condition in noise floor : RBW=VBW=100Hz*

Package Drawing



	MILLMETER		
SYMBOL	MIN	NOR	MAX
A	0.41	0.45	0.5
A1	0	0.02	0.05
D		1.1BSC	
E		0.7BSC	
e		0.4BSC	
L	0.15	0.25	0.35
L1	0	0.05	0.1
L3	0.15	0.2	0.25

Figure 12

Revision History

Table 7

Revision Number	Revision Date	Description	Modifications
0.0	2020/11/12	Draft	—
0.1	2020/12/10	Initial release	
0.2	2021/6/28	Release	
0.3	2021/9/27	Update	specification&application information
1.0	2021/11/27	Update	
1.1	2022/1/31	Update	Update figure
1.2	2022/5/26	Update	Update figure
1.3	2023/8/25	Update	Modify Figure7
1.4	2023/10/18	Update	Modify IIP3
1.5	2025/08/18	Update	Update General Description/Features/Specification/Pin Diagram/Typical Performance Characteristics/Application Circuit/Package Drawing

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

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